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DESIGN, IMPLEMENTATION AND TEST OF AN RS-232 COMPATIBLE BI-DIRECTIONAL, FULL DUPLEX, FIBER-OPTIC INTERFACE WITH PROVISION FOR HARDWARE HANDSHAKING ON A MINIMUM OF FIBER-OPTIC LINES

by

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The objective of this thesis research was the design and implementation of an RS-232 compatible, bi-directional, full duplex, fiber optic interface with provision for hardware handshaking. Results show that active handshaking lines can be successfully multiplexed, converted to light, transmitted, received, reconverted and demultiplexed pleisiochronously for data communications at 19.2 kilobaud. Use of wavelength division multiplexing and optical duplexing enable the reduction of individual fiber optic lines required from four uni-directional single frequency fibers to two bi-directional fibers at three operating wavelengths.

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ABSTRACT

The objective of this thesis research was the design and implementation of an RS-232 compatible, bi-directional, full duplex, fiber optic interface with provision for hardware handshaking. Results show that active handshaking lines can be successfully multiplexed, converted to light, transmitted, received, reconverted and demultiplexed pleisiochronously for data communications at 19.2 kilobaud. Use of wavelength division multiplexing and optical duplexing enabled the reduction of individual fiber optic lines required from four uni-directional single frequency fibers to two bi-directional fibers at three operating wavelengths.

TABLE OF CONTENTS

I. INTRODUCTION

A. PURPOSE

The purpose of this thesis research is multifold. First, it is an attempt to resolve a gap in the existing commercially-manufactured fiber optic (F/O) interface device market. Commercially available RS-232 fiber optic interface devices provide only for data transmission and reception. Examples are the ADC Fiber Optics Corporation Connectorized Active Full Duplex Coupler (CAF) [Ref. 1], the Hewlett Packard HFBR-0400 series of fiber optic receivers and transmitters [Ref. 2], and the Black Box Corporation TA-MD940B-M/F and TA-ME950/1-C fiber optic receivers and transmitters [Ref. 3]. None of the these devices provide for the implementation of hardware control (handshaking) between devices with RS-232 interfaces.

Second, it is an attempt to resolve this gap in a cost-effective off-the-shelf manner without complex and expensive electronics. There is, at present, an effort underway at Crystal Semiconductor Corporation [Ref. 4] to produce a chip which will incorporate a full set of multiplexed RS-232 handshaking lines with the transmission of the data. To quote their representative, "it is a complex digital machine" and, at its current stage of development, is "plagued by serious anomalies". The simpler approach used in this thesis

research is described with details of the number and types of control signals which can be incorporated.

Third, this thesis attempts to minimize the number of fiber optic lines necessary to implement the RS-232 interface through the use of wavelength division multiplexing (WDM) and optical duplexing. More efficient fiber usage enables cost, weight and volume reduction of the interconnect.

Last, this thesis highlights some of the obvious advantages of the use of fiber optic RS-232 interfaces for military applications.

B. CONCEPT

The concept for the design and implementation of this thesis was:

- Obtain two data terminals with RS-232 interfaces, connect these devices in a configuration which enables data transfer with active hardware handshaking, and analyze the data and handshaking lines to determine the format of those signals.
- Design a circuit which will convert RS-232 signal levels to transistor-to-transistor logic (TTL) levels required for interface with fiber optic receivers and transmitters.
- Design a circuit which will multiplex the control signals into a single signal for fiber optic transmission and conversely demultiplex the signals at the receiver.
- Choose fiber optic receiver/transmitter pairs to interface with previously designed circuitry.
- Determine a way to ensure that the transmit multiplexer and the receive demultiplexer are synchronized (or nearly so) so that handshake signals appear on their correct outputs.
- Implement the design and test transmission via as many fibers as are required by the design.

- Reduce the number of fibers through the use of WDM techniques and optical duplexing techniques.

Figure 1 shows a block diagram of this concept. Figure 2 shows a more detailed functional block diagram of the implementation concept.

C. SUMMARY OF RESULTS

The results of the thesis research are summarized as follows:

- The Hewlett Packard-150 (HP-150) Personal Computer was chosen for both the host and the remote terminal for the data transfer. The device has an RS-232 interface, the handshaking and data lines are easily accessible and there is a tailored software package for file transfer. Detailed information on interface and configurations is available in Chapter II.

- The MAX232, +5V powered, dual, RS-232 transmitter/receiver was used to convert the RS-232 voltages to TTL level signals and vice versa. The MAX232 integrated circuits (IC's) were provided by NPS Optical Electronics Lab Technician John Glenn. Description of IC operation is provided in Chapter III.

- A multiplex/demultiplex circuit was designed and is described in detail in Chapter III. Refinements, enhancements and expansion of the circuit are also discussed in Chapter VI.

- The ADC CAF and the HP 0400 series of fiber optic receiver/transmitters were employed. Details of transmission/reception of signals at optical wavelengths are provided in Chapter II.

- A pleisiochronous interface was designed (based on a suggestion by John Glenn) which uses the transmitted data to synchronize the multiplexing and demultiplexing of the control signals. The circuit is described in detail in Chapter III.

- A test was conducted which showed that a 15000 byte binary file could be transmitted at 19.2 kilobaud over three fiber optic cables (one for data transmit and receive, one for control transmit and one for control receive). The file was transferred with no errors.

Active handshaking lines were multiplexed, transmitted, received and demultiplexed successfully. Test procedures and results are detailed in Chapters IV and V.

- Use of fiber optic (F/O) duplexing and WDM enabled the number of fibers for this interface to be reduced to two fibers instead of the four fibers required if no WDM or duplexing had been used. WDM and optical duplexing, as applicable to this thesis, are described in Chapter II. The test of the interface was conducted successfully over two fibers.

- Theoretical analysis of potential link lengths has been developed and is found in Chapter VI.

- Possible refinements and ideas for future topics are presented in Chapter VI and VII.

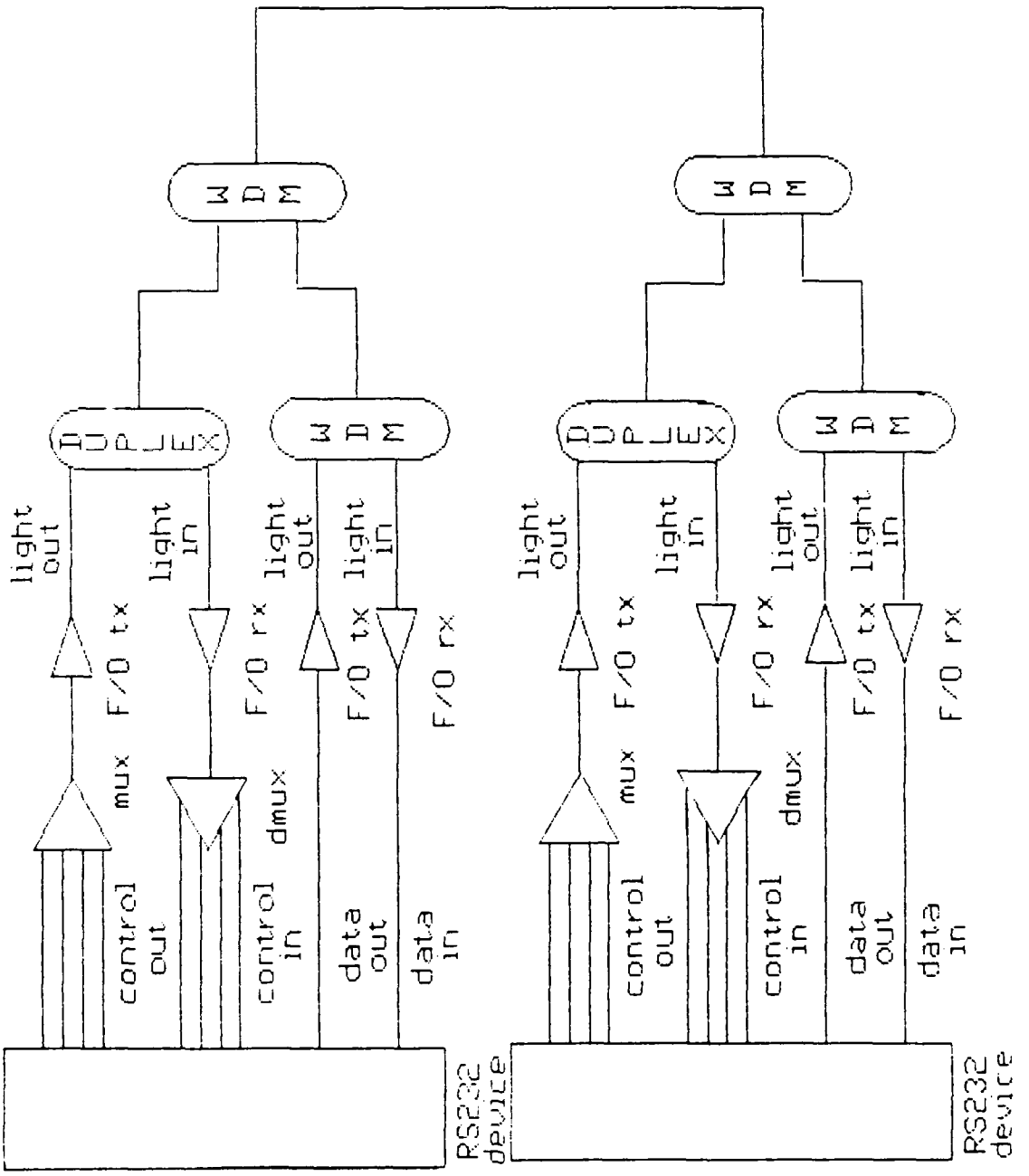


Figure 1. Implementation Concept Diagram

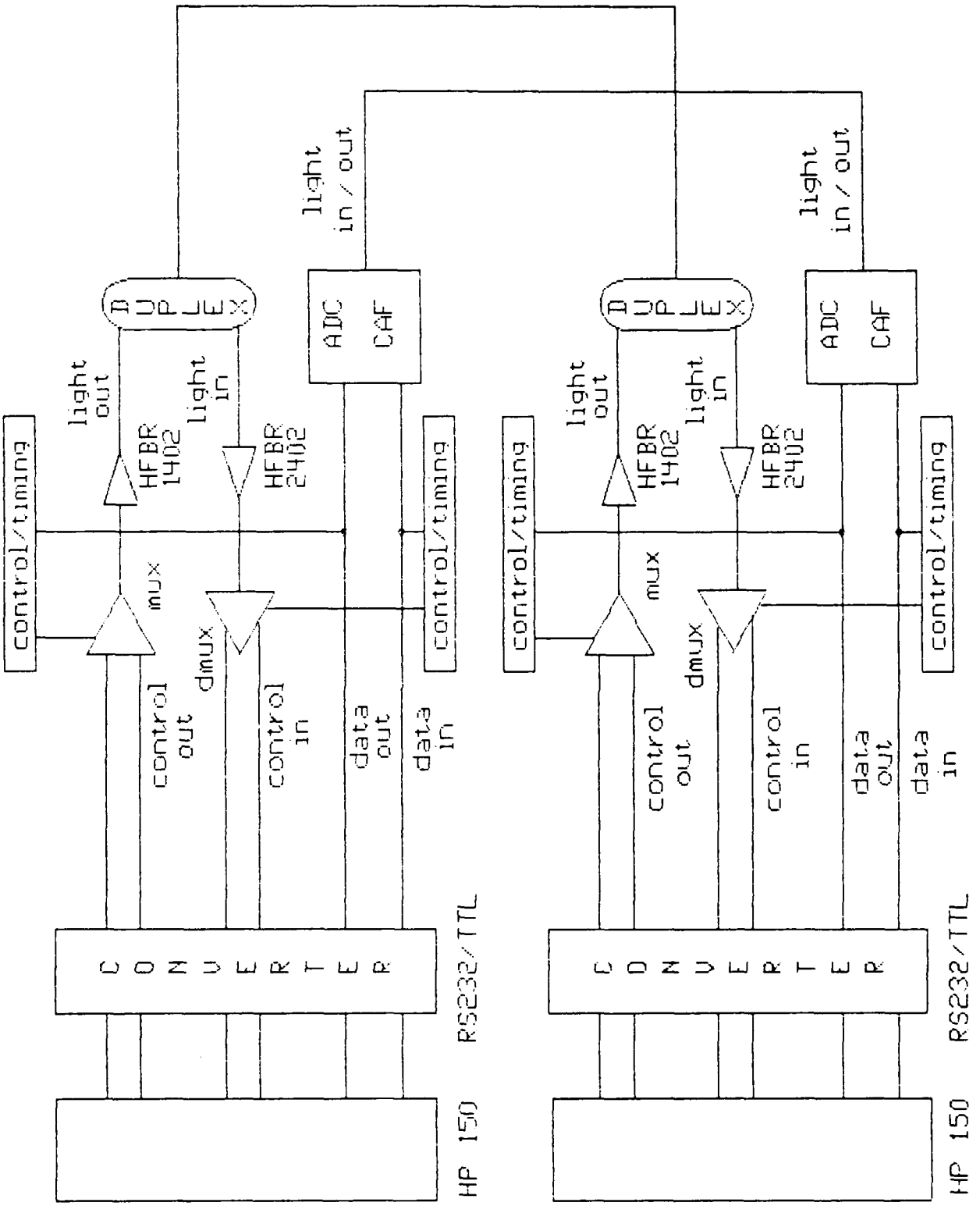


Figure 2. Functional Block Diagram

II. BACKGROUND

A. TERMINAL DEVICES

This section addresses specifics of the Hewlett Packard-150 (HP-150) Personal Computer, including details of its operation, configuration and data transfer capability.

The HP-150 is a personal computer which can function as a stand-alone computer, a remote terminal, or a host terminal. [Ref. 5] As a terminal, the HP-150 can communicate remotely with a computer or process data autonomously [Ref. 6]. For this thesis research, the HP-150s have been configured to act as a link station and a monitor (host) station for the purpose of transferring data files. Two HP communications programs, Distributed Systems Network (DSN) Link and DSN Monitor, were employed to enable communications and data file transfer between the two PCs [Ref. 7].

General installation, connection and start-up details for the HP-150 are provided in Reference 5. The key information for configuring the two HP-150 PCs for data transfer using the Link and Monitor Programs has been extracted from References 5, 6 and 7 and is delineated herein:

1. Insert disc with operating system and device configuration into drive A and turn on HP-150. Select the "device configuration" application and press "start application". Insure that the "Main" configuration screen is identical to Figure 3. Changes to all of the configuration

screens, if needed, are made as described in References 5, 6 and 7.

2. Press "User System" twice on the HP-150 keyboard and select "configure keys" from the soft key menu at the bottom of the screen.

3. Next select "global configuration" from the soft key menu and insure that the global configuration is identical to Figure 4.

4. Select "configure keys" (soft key menu) and then "port 1 configuration" (also soft key menu). Insure that the port 1 configuration is identical to Figure 5.

5. Select "configure keys" and "terminal configuration" and insure that the terminal configuration screen is identical to Figure 6.

6. When all configurations have been completed, press "control", "shift", "reset" simultaneously on the HP-150 keyboard to return to the original applications screen.

7. Repeat 1-6 above for the other HP-150.

8. Insert DSN/Link and DSN/Monitor discs (one into each HP-150) and select soft key "reread discs". When the application screens appear, select soft key "start application" on each terminal.

9. On the DSN/Link terminal, select "transfer to host" from the soft key menu and the screen of Figure 7 will appear on the "link" terminal with the screen of Figure 8 appearing on the "monitor" terminal. Fill in the "link" terminal

screen prompts (Local Source File and Host Destination File). (Note: the local source file must exist on the disc in drive A or B on the "link" terminal. The destination file name is somewhat arbitrary, but must be the same file type as the source file.)

10. Select soft key "start transfer" on the "link" terminal. At the completion of file transfer the terminal screens should appear as shown in Figure 9 for the "link" terminal and as shown in Figure 10 for the "monitor" terminal. If file transfer is unsuccessful an error message will appear on both the "link" and the "monitor" terminals.

11. During the configuration and file transfer procedure described above, the PCs were directly connected from interface port, "port 1", to the distant interface port, "port 1", via the null modem wiring configuration. The null modem connections are described in detail in the following section. The interface port, "port 1" is the 25-pin female RS-232 connector whose location is shown in Figure 11.

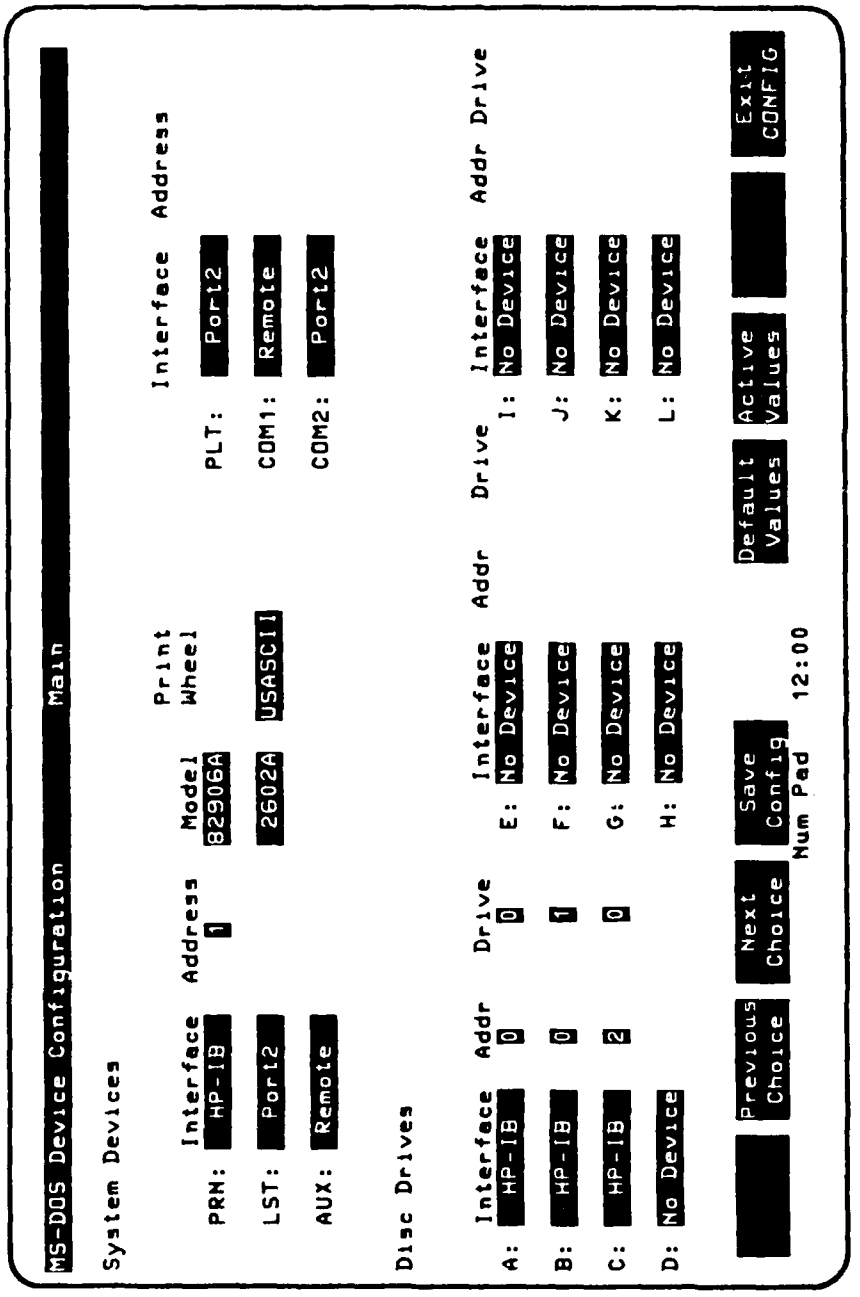


Figure 3. "MAIN" Configuration Screen
[from Ref. 5:p. A-23]

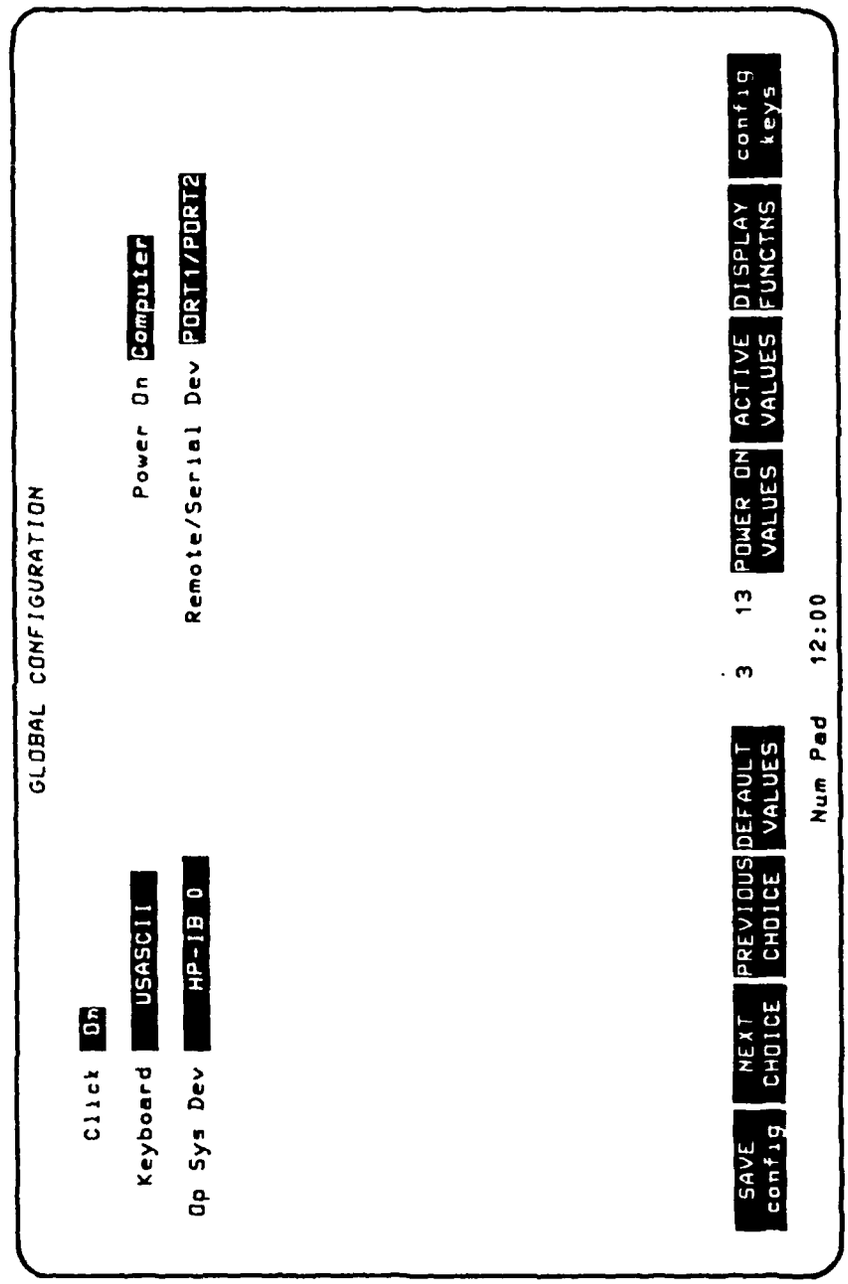


Figure 4. "GLOBAL" Configuration Screen
[from Ref. 5:p. A-3]

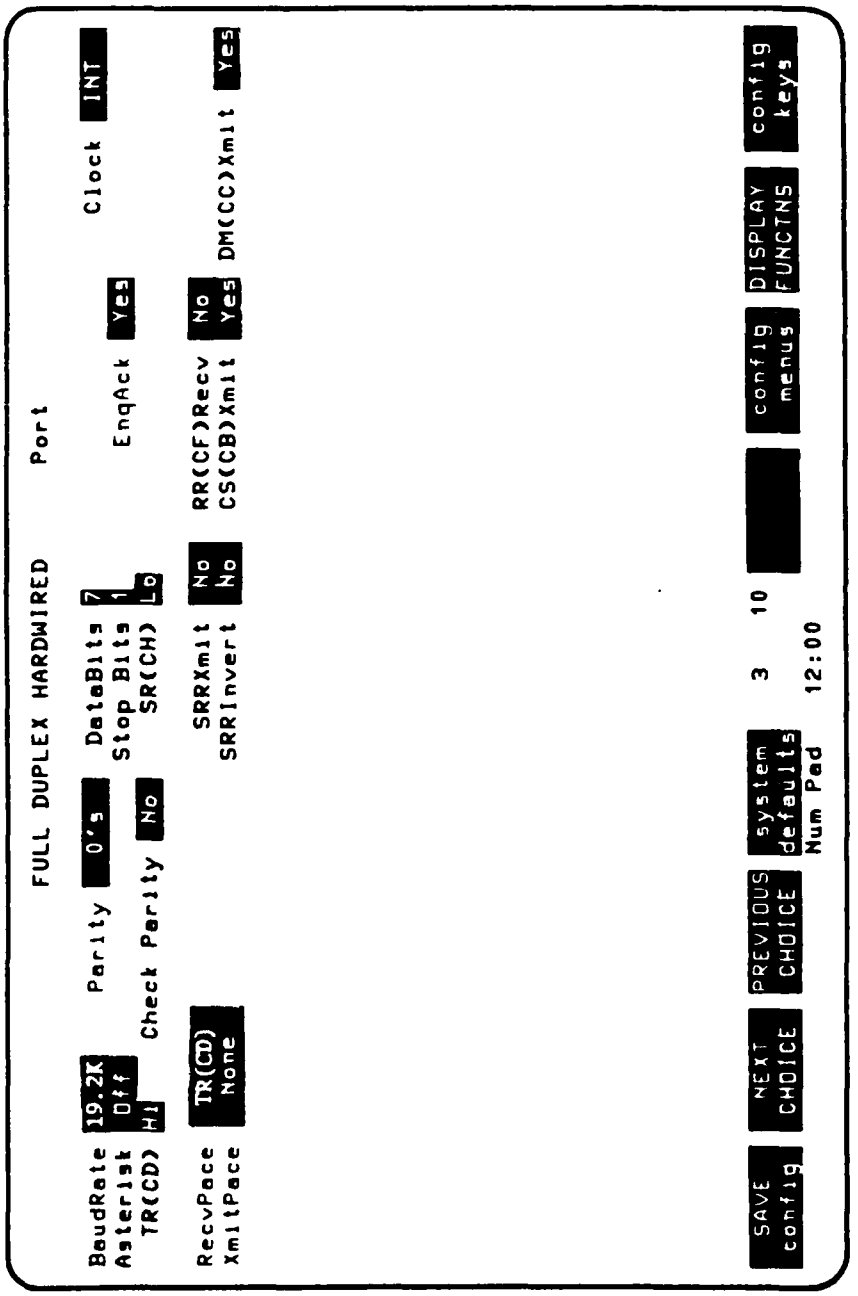


Figure 5. "PORT 1" Configuration Screen
[from Ref. 5:p. A-5]

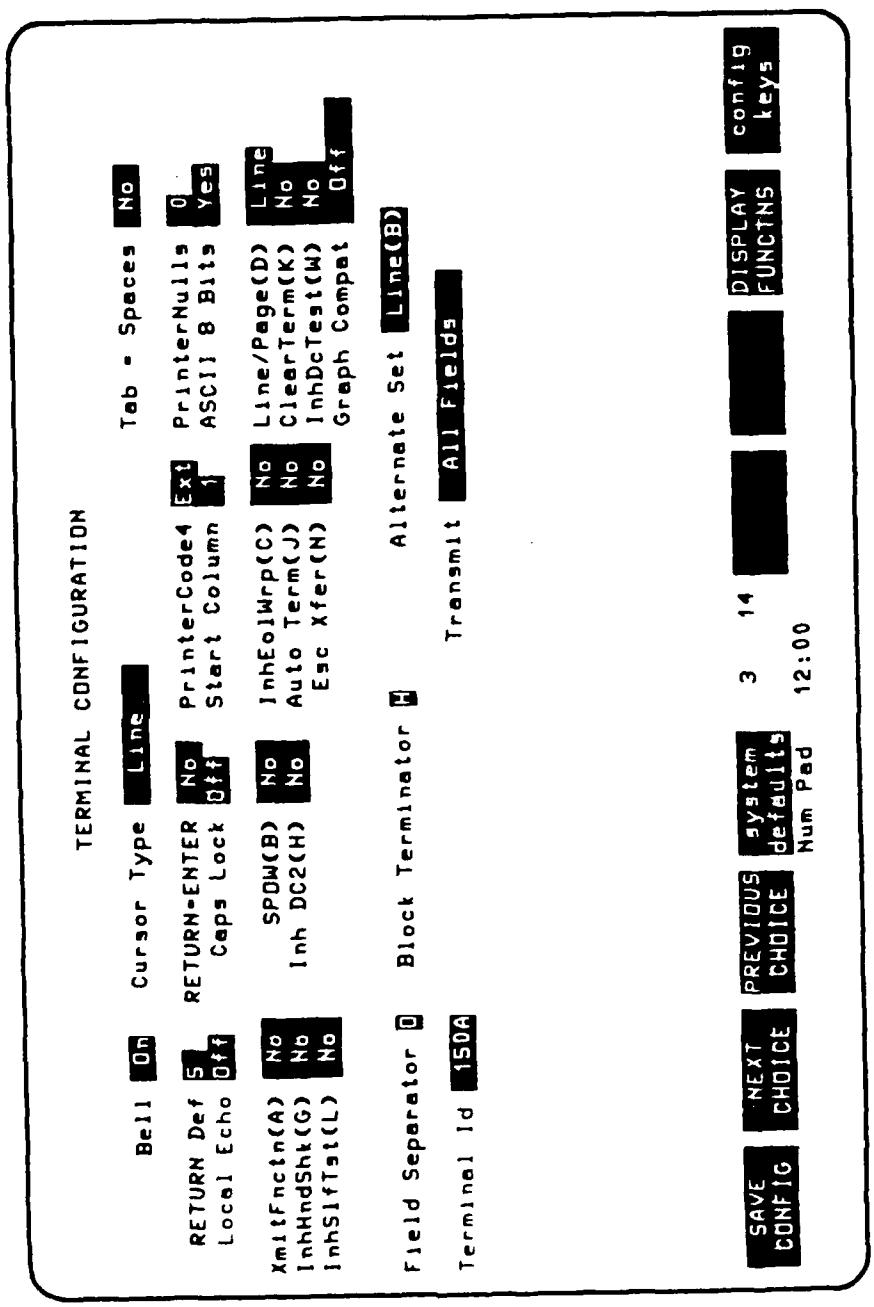


Figure 6. "TERMINAL" Configuration Screen [from Ref. 5:p. A-14]

Figure 7. "LINK" Menu Screen
[from Ref. 7:p. 5-3]

Figure 8. "MONITOR" Waiting Transfer Screen
[after Ref. 7, Advanced Link Supplement:p. 10]

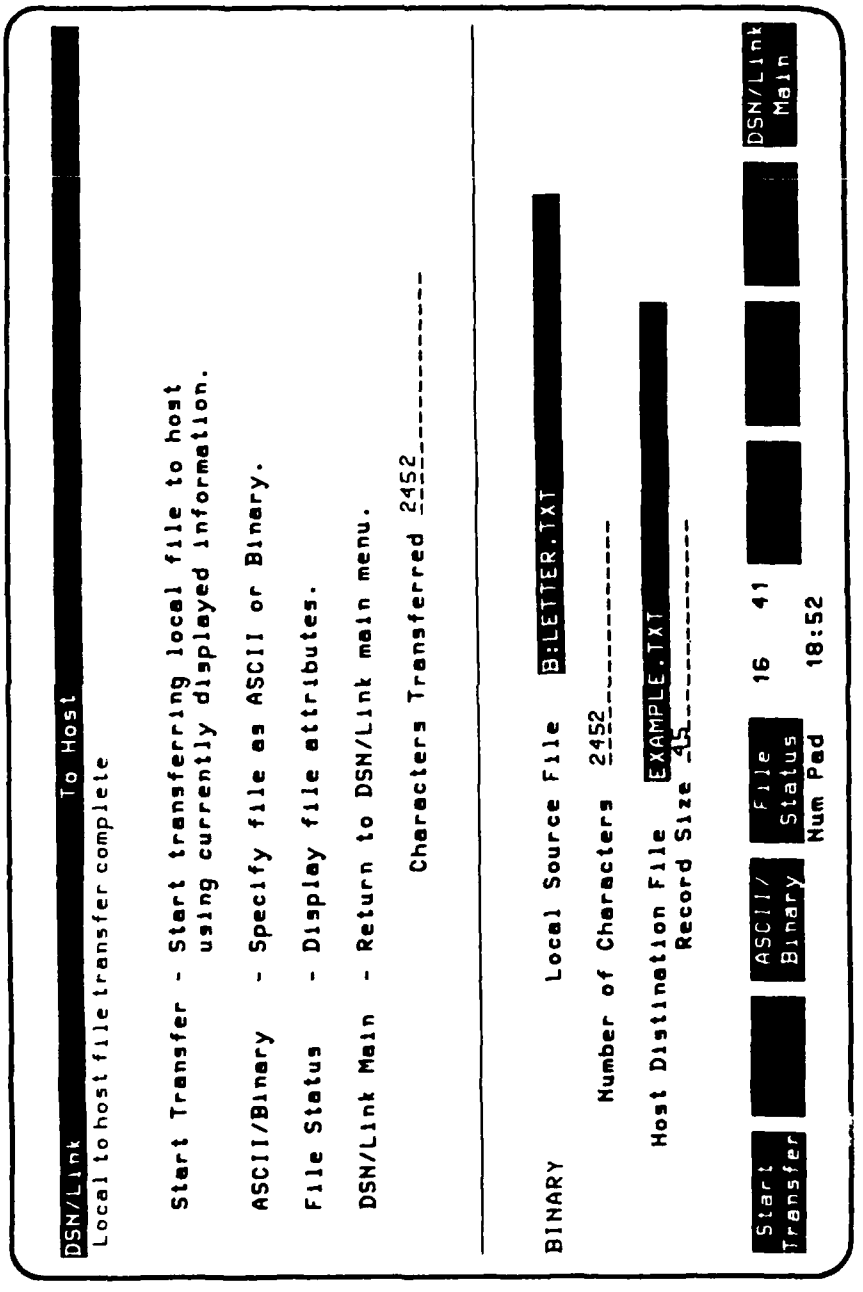


Figure 9. "LINK" Transfer Complete Screen
[after Ref. 7:p. 4-3]

Figure 10. "MONITOR" Transfer Complete Screen
[after Ref. 7, Advanced Link Supplement:p. 10]

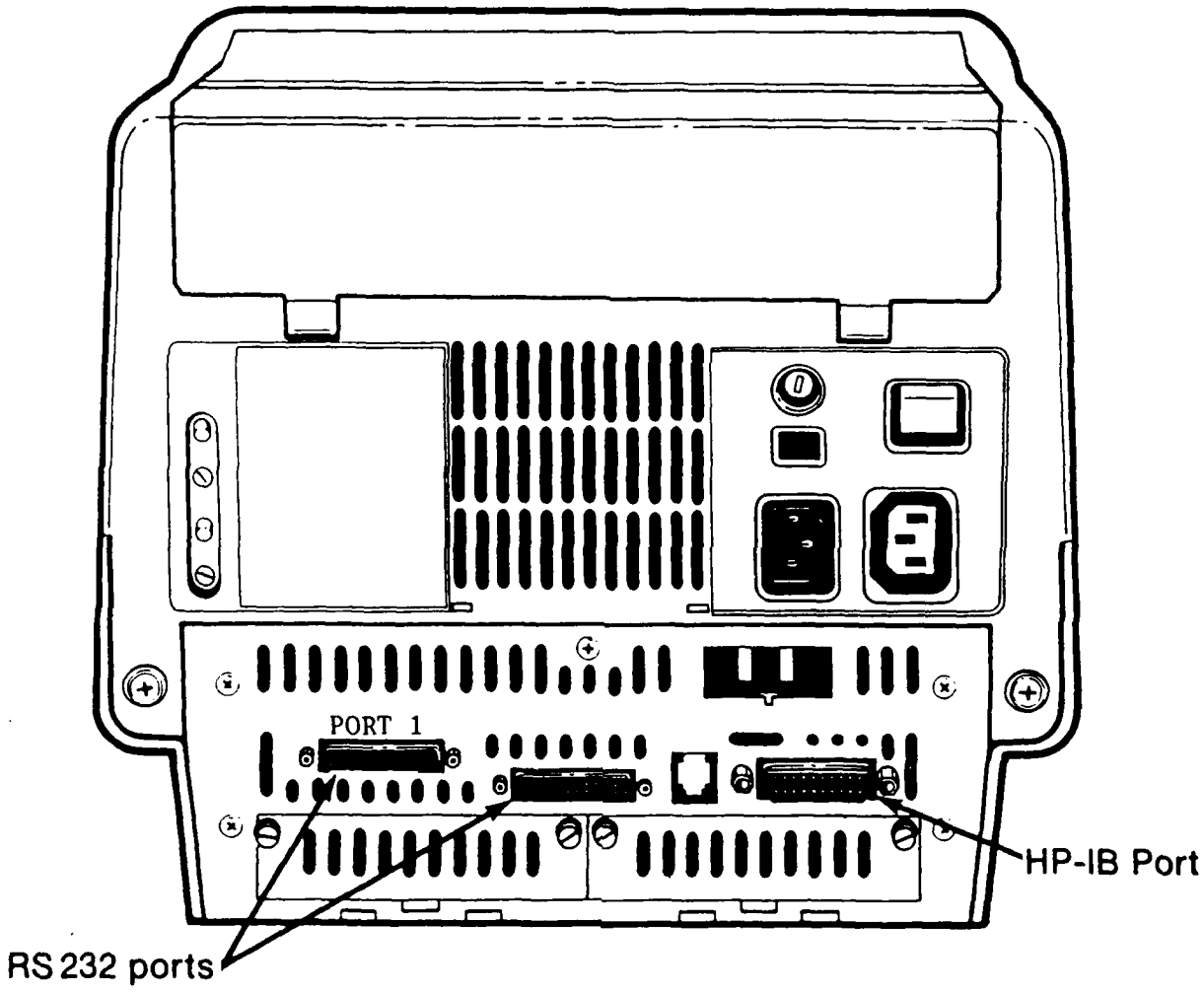


Figure 11. "PORT 1" RS-232 Interface Location
[from Ref. 5:p.3-16]

B. RS-232 INTERFACE

This section describes the RS-232 interface in general, including mechanical and electrical details as well as drawbacks and peculiarities of the interface. It also describes specifically the RS-232 interface used for data transfer in this research.

One common interface between computer equipment and peripheral equipment is the serial interface. Specifically, the transmitter sends each character, or group of bits, one bit at a time over a single line. The receiver detects each incoming bit and reassembles the bits into the transmitted character. Each transmitted character is preceded by a start bit and followed by a stop bit. The start and stop bits separate each character from the next. An optional parity bit may precede the stop bit. The parity bit is used to check the accuracy of transmission. The data bits and the start, stop and parity bits are transmitted in a group known as a frame. [Ref. 8:pp. 398-400]

The Electronic Industries Association (EIA) has attempted to standardize the serial interface's electrical and mechanical characteristics. The resulting standard is known as the RS-232C Serial Interface Standard. The RS-232C standard as developed by the EIA is intended to link data terminal equipment (DTE) with data communications equipment (DCE). By this standard, DTE refers to the computer or

terminal and DCE to the line equipment or modem. [Ref. 9:p. 10]

The mechanical details of the EIA RS-232C interface are shown in Figure 12. The pin functions of the 25 pin connector established by the EIA standard are listed in Table 1. It is important to note that some of these pin functions such as data carrier detect and ring indicator are peculiar only to the modem-to-modem telephone communication aspects of the interface. They are not implemented in many defacto uses of the RS-232C interface that are not covered specifically by the EIA standard. The electrical characteristics of the EIA RS-232C serial interface are shown in Table 2. As can be seen from Table 2, the length and data rate of the RS-232C interface are quite limited. Use of fiber optic interconnect facilities, such as the one researched by this thesis, offers a substantial improvement in the maximum distance and data rate of an RS-232C interface.

The mechanical details of the standard are adhered to by the majority of equipment suppliers. However, in order to interconnect equipment not specifically addressed by the EIA RS-232C standard, manufacturers commonly implement their own unique subset of the RS-232C interface [Ref. 8:p. 422]. For this thesis, one such subset, the null modem interface, is implemented to enable HP-150-to-HP-150 data communications.

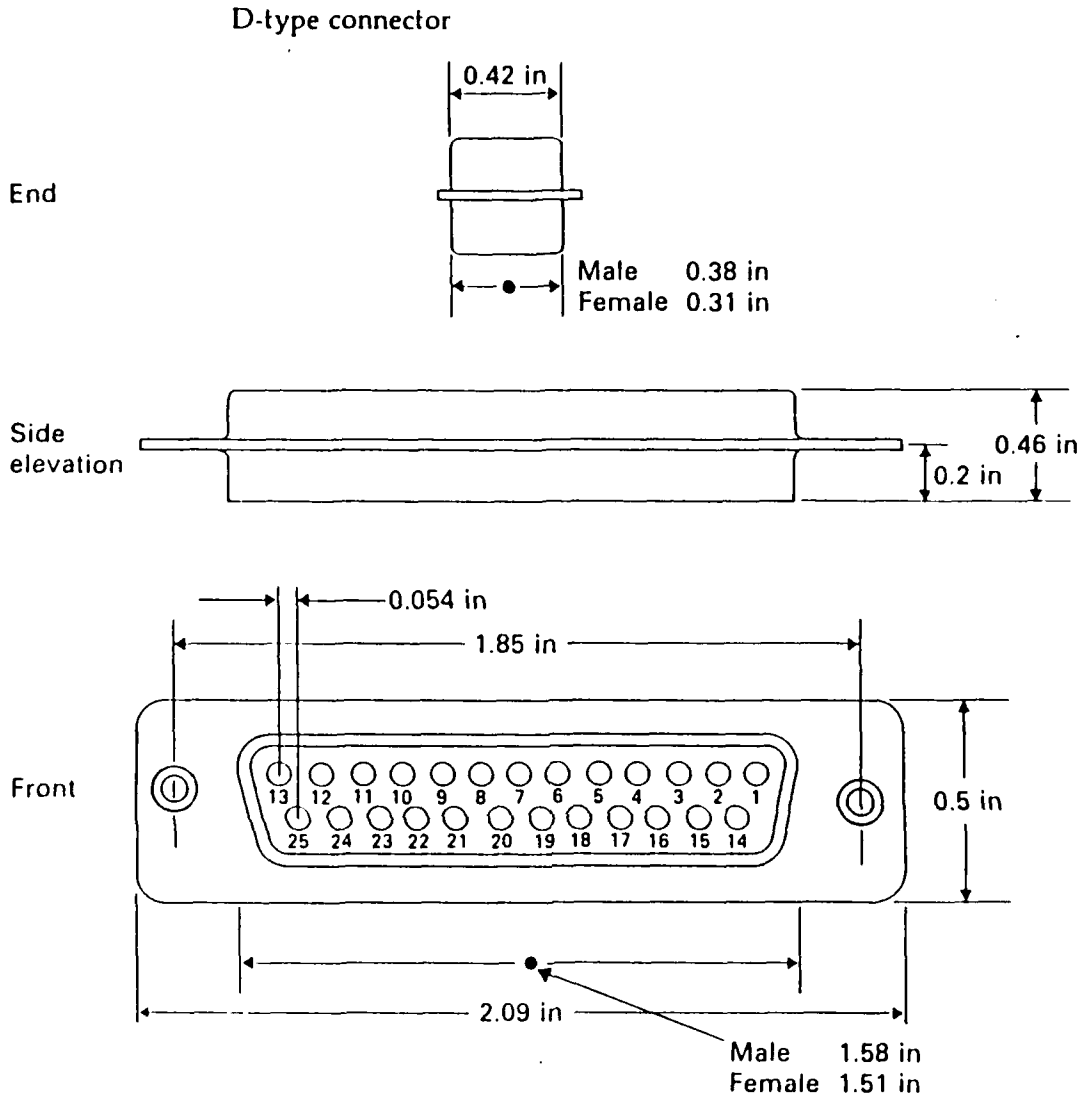


Figure 12. RS-232 Mechanical Interface
[from Ref. 8:p. 423]

TABLE 1
(EIA) RS-232 PIN FUNCTIONS
[from Ref. 8:p. 424]

PIN	NAME	FUNCTION
1	Protective ground	Electrical equipment frame and d.c. power ground
2	Transmitted data	Serial data generated by the DTE
3	Received data	Serial data generated by the DCE
4	Request to send	When asserted indicates that the DTE is ready to transmit primary data
5	Clear to send	When asserted indicates that the DCE is ready to transmit primary data
6	Data set ready	When asserted indicates that the DCE is not in a test, voice, or dial mode, that all initial handshake, answer tone, and timing delays have expired
7	Signal ground	Common ground reference for all circuits except protective ground
8	Received line signal detector	When asserted indicates that carrier signals are being received from the remote equipment
9	Reserved	
10	Reserved	
11	Unassigned	
12	Secondary received line signal detector	When asserted indicates that the secondary channel data carrier signals are being received from the remote equipment
13	Secondary clear to send	When asserted indicates that the DCE is ready to transmit secondary data
14	Secondary transmitted data	Low-speed secondary data channel generated by the DTE
15	Transmitted signal element timing	The signal on this line provides the DTE with signal element timing information
16	Secondary received data	Low-speed secondary channel data generated by the DCE
17	Receiver signal element timing	The signal on this line provides the DTE with signal element timing information
18	Unassigned	
19	Secondary request to send	When asserted indicates that the DTE is ready to transmit secondary channel data
20	Data terminal ready	When asserted indicates that the data terminal is ready
21	Signal quality detector	When asserted indicates that the received signal is probably error free; when negated indicates that the received signal is probably in error
22	Ring indicator	When asserted indicates that modem has detected a ringing tone on the telephone line
23	Data signal rate detector	Selects between two possible data rates
24	Transmit signal element timing	The signal on this line provides the DCE with signal element timing information
25	Unassigned	

TABLE 2
RS-232 ELECTRICAL INTERFACE CHARACTERISTICS
[from Ref. 8:p.425]

CHARACTERISTIC	VALUE
Operating mode	Single ended
Maximum cable length	15 m
Maximum data rate	20 kilobaud
Driver maximum output voltage (open-circuit)	$-25\ V < V < +25\ V$
Driver minimum output voltage (loaded output)	$-25\ V < V < -5\ V$ OR $+5\ V < V < +25\ V$
Driver minimum output resistance (power off)	300 Ω
Driver maximum output current (short-circuit)	500 mA
Maximum driver output slew rate	30 V/μs
Receiver input resistance	3–7 kΩ
Receiver input voltage	$-25\ V < V_i < +25\ V$
Receiver output state when input open-circuit	Mark (high)
Receiver maximum input threshold	−3 to +3 V

In order to design a serial interconnection between two HP-150 PCs, it is necessary to determine how the RS-232 interface is implemented for these devices. As previously stated, the RS-232C standard was developed for interface between Data Terminal Equipment (DTE) and Data Communication Equipment (DCE) (i.e., a modem). Since the computer-to-computer connection is not covered by the standard interface, the "standard" must be customized for this use. [Ref. 9:pp. 19-20]

One defacto use of an RS-232 interconnection with control lines between a peripheral and a computer is shown in Figure 13. (Outputs are marked with ! and inputs with ?.) DTEs

transmit data on pin 2 and receive data on pin 3. DCEs transmit data on pin 3 and receive data on pin 2. [Ref. 9:p. 20]

Figure 14 shows the specifics of the RS-232C port 1 connector of the HP-150s employed in this research. Table 3 provides the key to the pin identifiers. As can be seen, the HP-150 transmits on pin 2 and receives on pin 3. Therefore, it must be considered to be a DTE.

A common method of connecting two DTEs is known as the "null modem configuration" [Ref. 10:p. 38] which is shown in Figure 15. The null modem configuration is employed for this thesis. An HP technical representative provided the information that the DSN Link/Monitor interconnect could be implemented successfully using the null modem configuration.

The specific levels and directions on the HP-150 handshaking and data lines are as follows:

1. Pin 1, common, shield ground
2. Pin 2, data, output, -10V idle, +/-10V active
3. Pin 3, data, input
4. Pin 4, RTS, output, +10V asserted/-10V negated
5. Pin 5, CTS, input
6. Pin 6, DSR, input
7. Pin 7, common, signal ground
8. Pin 20, DTR, output, +10V asserted/-10V negated

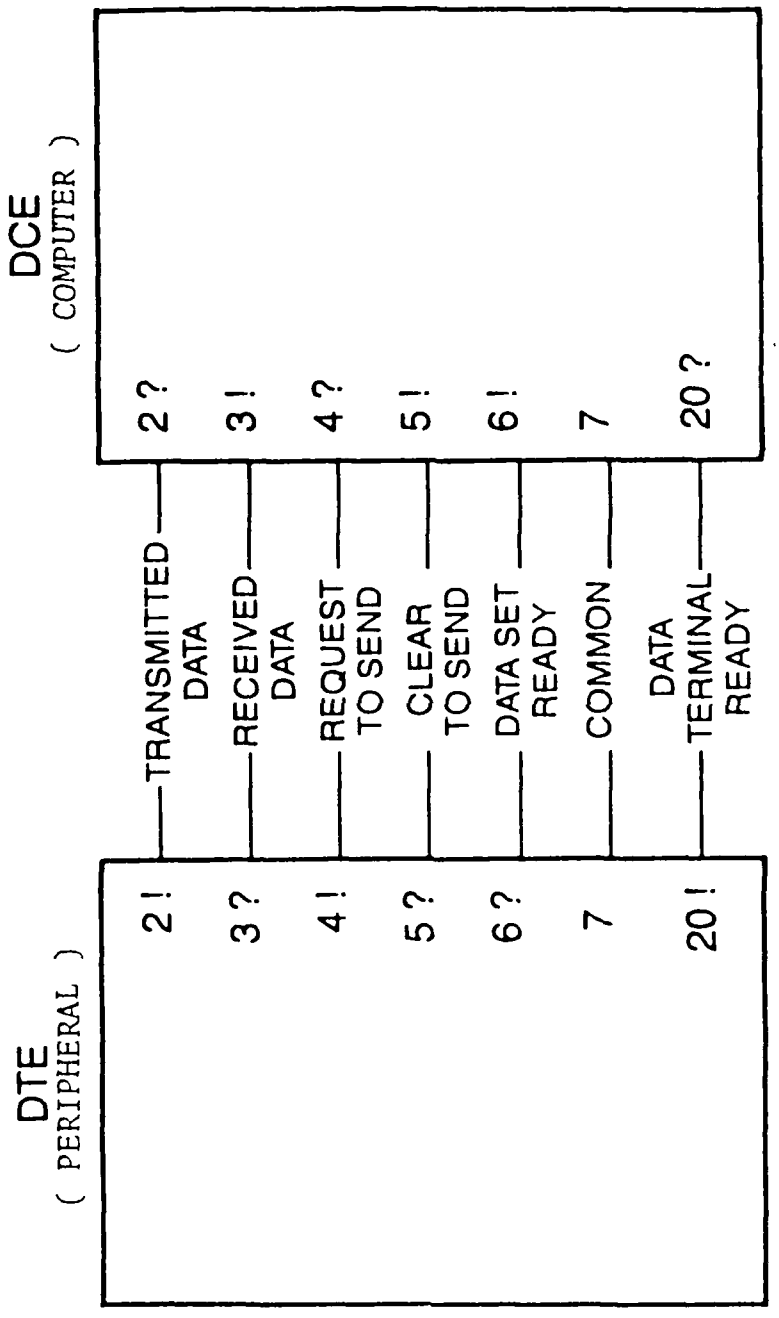


Figure 13. Adaptation of the RS-232C Serial Interface Standard to Connect a Peripheral and a Computer [from Ref. 9:p. 42]

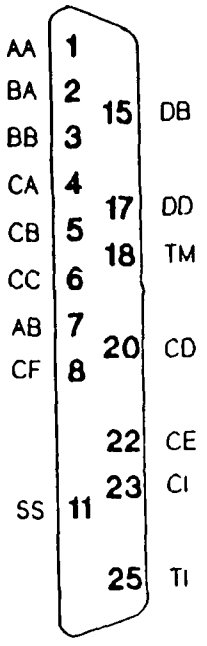


Figure 14. HP 150 RS-232 Port 1, pin connections [from Ref. 7:p. 9]

TABLE 3.
KEY TO FIGURE 14 [Ref. 7:p. 9]

AA	Cable shield
AB	Signal ground
BA	Transmitted data
BB	Received data
CA	Request to send
CB	Clear to send
CC	Data set ready
CD	Data terminal ready
CE	Ring indicator
CF	Received line signal detector
CI	Data signal rate (DCE source)
DA	Transmitter signal element timing (DTE source)
DB	Transmitter signal element timing (DCE source)
DD	Receiver signal element timing
SCA	Secondary request to send
SCF	Secondary received line signal detector
SS	Select standby
TI	Test indicator
TM	Test mode

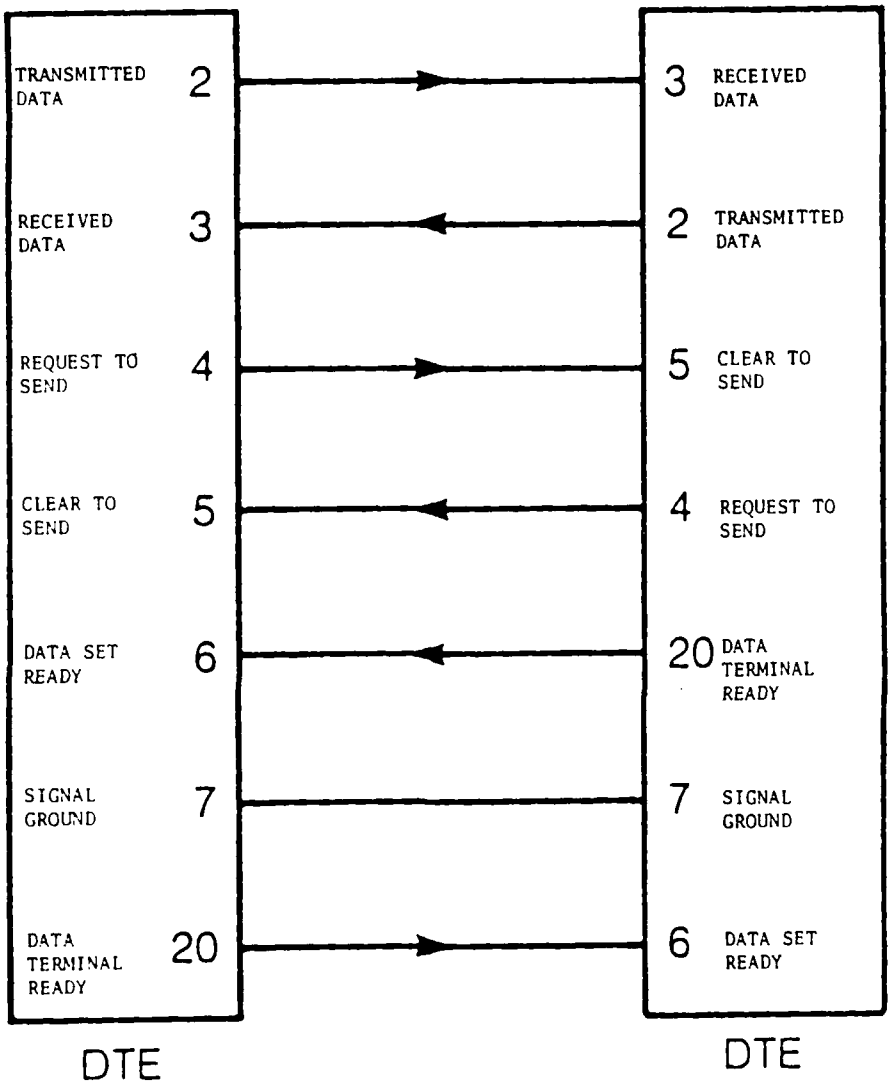


Figure 15. Null Modem Configuration
[from Ref. 10:p. 269]

In the fiber optic interconnect designed for this thesis, pin 1 and pin 7 were grounded locally. Pin 1 or shield ground (sometimes known as protective ground or chassis ground) is used to connect two pieces of equipment which are powered by different distribution feeders with different electrical paths to earth ground. This pin 1 to pin 1 connection is intended to alleviate problems where the chassis ground on each piece of equipment is not identical. In many cases, however, this connection causes its own peculiar problem known as a "ground loop". [Ref. 9:p. 58] Figure 16 and Figure 17 depict two possible grounding configurations which may result in ground loop problems.

Figure 16 shows a complete loop from ground on chassis A through the ground on chassis B. Changing fields in cables carrying AC current in proximity to the equipment or lightning strikes can induce a potential across the loop causing a current to flow therein. Since the loop impedance is low, this current can be very high even for a few volts potential difference and can cause damage to the equipment.

Figure 17 shows an electrically safe ground loop (i.e., damage to equipment is not likely to result from ground loop currents) but residual current flow in the loop induced by various signal and power cabling is likely to result in a noise voltage which may affect the signal voltage to noise voltage ratio adversely. [Ref. 11:pp.43-45]

One of the major advantages of the use of the fiber optic RS-232 interface designed in this thesis is elimination of the ground loop problem. Other advantages are discussed in detail in Chapter VI.

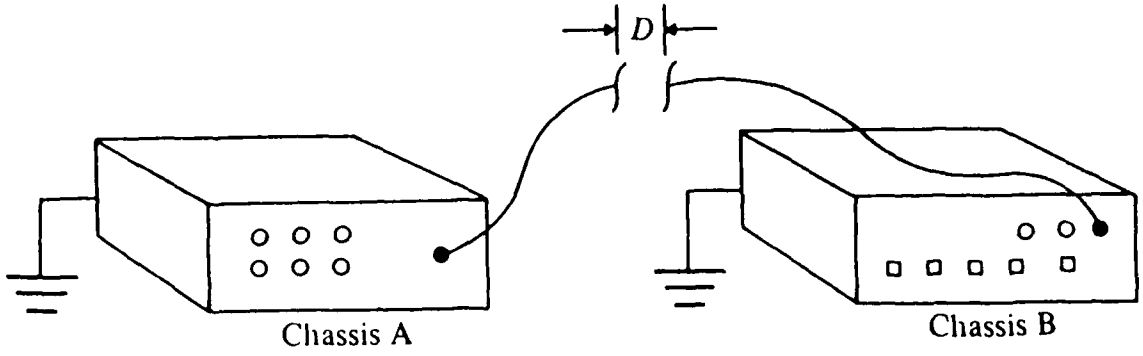


Figure 16. Ground Loop Example A
[from Ref. 11:p. 44]

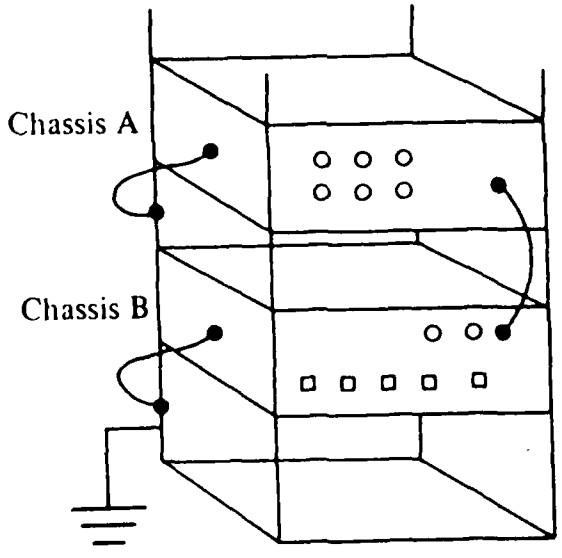


Figure 17. Ground Loop Example B
[from Ref. 11:p. 44]

C. CIRCUIT DESIGN PHILOSOPHY

The previous sections covered the selection of computers with an RS-232 interface, configuration of the computers for file transfer and characterization of the data and control signals to be transmitted and received. A method for RS-232-to-optical signal conversion and for reconversion of optical signals to RS-232 signals must now be determined.

The RS-232-to-optical signal interface circuit must perform the following functions:

1. RS-232-to-TTL signal conversion
2. Control signal multiplexing
3. Data signal (TTL levels) to optical signal conversion
4. Control signal (TTL levels) to optical signal conversion
5. Optical signal transmission and reception
6. Data signal optical-to-TTL conversion
7. Control signal optical-to-TTL conversion
8. Control signal demultiplexing
9. TTL-to-RS-232 signal conversion

Circuit operation is envisioned as follows:

The RS-232 voltage levels (+10V, -10V) are converted to TTL levels. The transmitted data signal from Pin 2 is converted to TTL and then taken directly to a fiber optic transmitter, converted to an optical signal and transmitted. The data signal on the transmit data line is used to activate the control line multiplexer. The output control signals (Pin 4, Request To Send, and Pin 20, Data Terminal Ready) are multiplexed together, converted to optical signals and transmitted. One fiber optic (F/O) transmitter is used to

transmit data signals, another one is used to transmit control signals.

At the receive side, two separate optical detectors receive the incoming optical signals and convert them to TTL levels. The incoming data signal is sent to Pin 3 (Receive Data) on the distant DTE after conversion to RS-232 levels. The TTL receive data signal is also used to activate the control line demultiplexer. The multiplexed TTL control signals are demultiplexed, converted to RS-232 levels and routed to the input control lines (Pin 5, Clear To Send, and Pin 6, Data Set Ready). Operation in the reverse direction mirrors the above description.

The design objectives which apply primarily to the multiplexing and demultiplexing of the control signals are listed below:

1. Easily available, off-the-shelf, proven performance components were desired.

2. Software intensive solutions, such as use of microprocessor control, were not desired.

3. Hardware intensive solutions, such as multiplex/demultiplex synchronization through clock recovery using Manchester encoding were not desired.

For the above reasons, the circuit design chosen was a pleisiochronous interface utilizing easily available hardware. The interface is described in Chapter III. The following considerations apply to the interface design:

- Control signals which are multiplexed on the transmitter side of the interface must be demultiplexed at the receiver side. These

signals should appear on the correct control inputs at the distant HP-150.

- The selection of the multiplex channels and demultiplex channels must be synchronized, or nearly so, to cause mutliplexed signals to appear on the correct channels after demultiplexing.

- Since the multiplexer clock and the demultiplexer clock are not in phase, "glitches" are expected to appear in the demultiplexed control signals as a result of the inability to start multiplexing and demultiplexing simultaneously. These "glitches" must be accommodated or eliminated.

- Circuit components which are not reliably initialized during "power-up" of the transmitter and receiver required a power-on, reset signal.

- "Deadlock" conditions where both HP-150s are awaiting control signals from the other must be avoided.

Each of the above design considerations is accounted for in the circuit design described in Chapter III or in enhancements of the design described in Chapter VI.

Block diagrams of the circuit implementation concept were previously shown in Figures 1 and 2. A detailed functional block diagram is shown in Figure 18. Specifics of each circuit component and its operation are given in Chapter III.

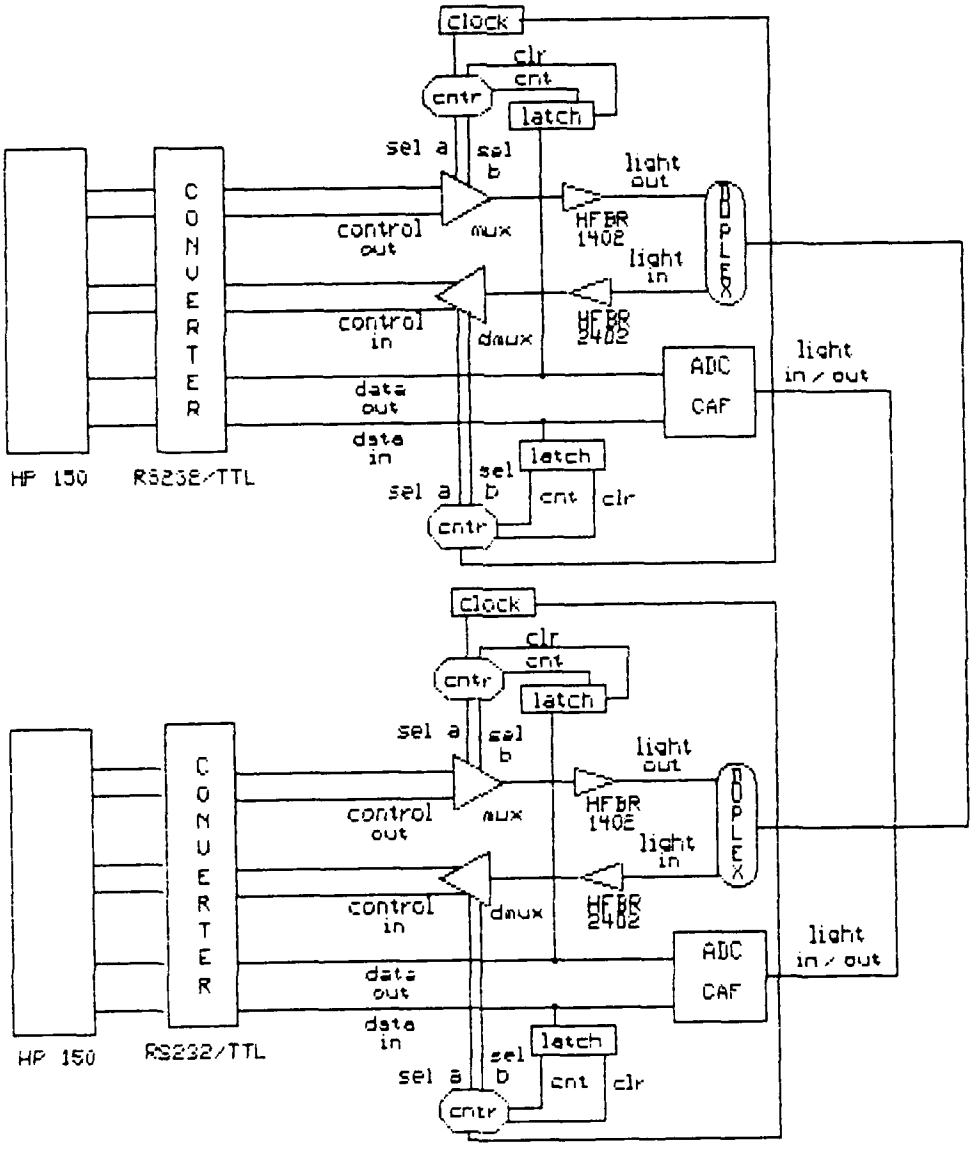


Figure 18. Detailed Functional Block Diagram

D. FIBER OPTIC EQUIPMENT

This section describes the F/O transmitters and receivers selected for use in this thesis research.

1. The Connectorized Active Full Duplex Couplers (CAFs) were purchased from ADC Fiber Optics Corporation as a Fiber Optics Transceiver Evaluation Kit. The CAF features an optical wavelength division coupler which combines and separates two optical wavelengths, allowing bi-directional optical transmission/reception.

The CAF modules operate from a single +5V supply and interface at TTL levels. A block diagram of the functional areas of the CAF is shown in Figure 19. The dichroic mirror arrangement which accomplishes the wavelength combination and separation is discussed in more detail in the following section.

The CAF transmitter circuit, shown in Figure 20, modulates an LED with the input data. The receiver circuit, depicted in Figure 21a, amplifies the PIN diode response to the optical signal to create a TTL-level output signal. The circuit shown in Figure 21b creates the -5V rail for the differential amplifier in the receiver circuit. A more detailed description of the operation of these circuits is provided in Reference 1. A pictorial comparison of a data link employing standard simplex F/O transmitter/receiver pairs with a data link employing a CAF is shown in Figure 22. [Ref. 1]

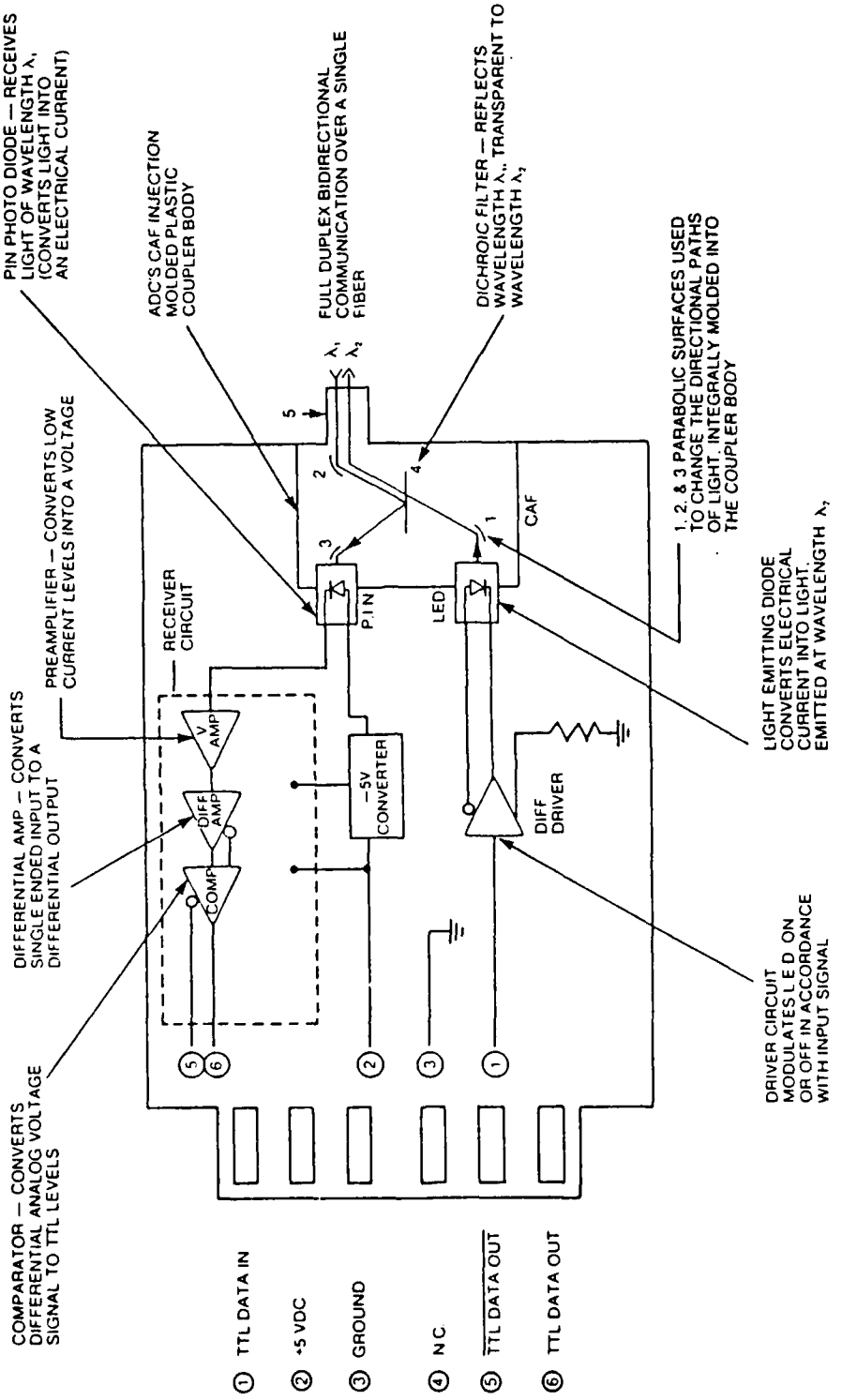


Figure 19. CAF Functional Areas
[from Ref. 1:p. 3]

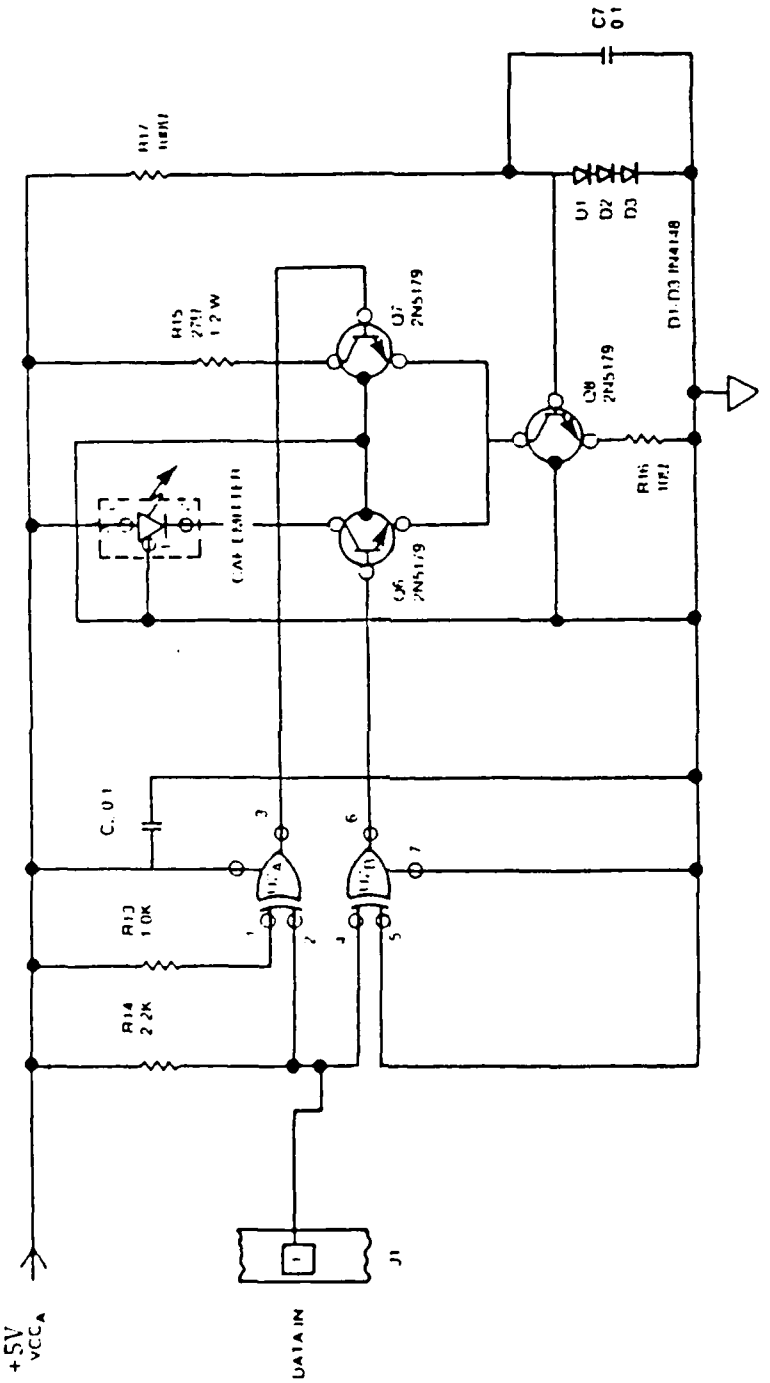


Figure 20. CAF Transmitter Circuit
[from Ref. 1:p. 7]

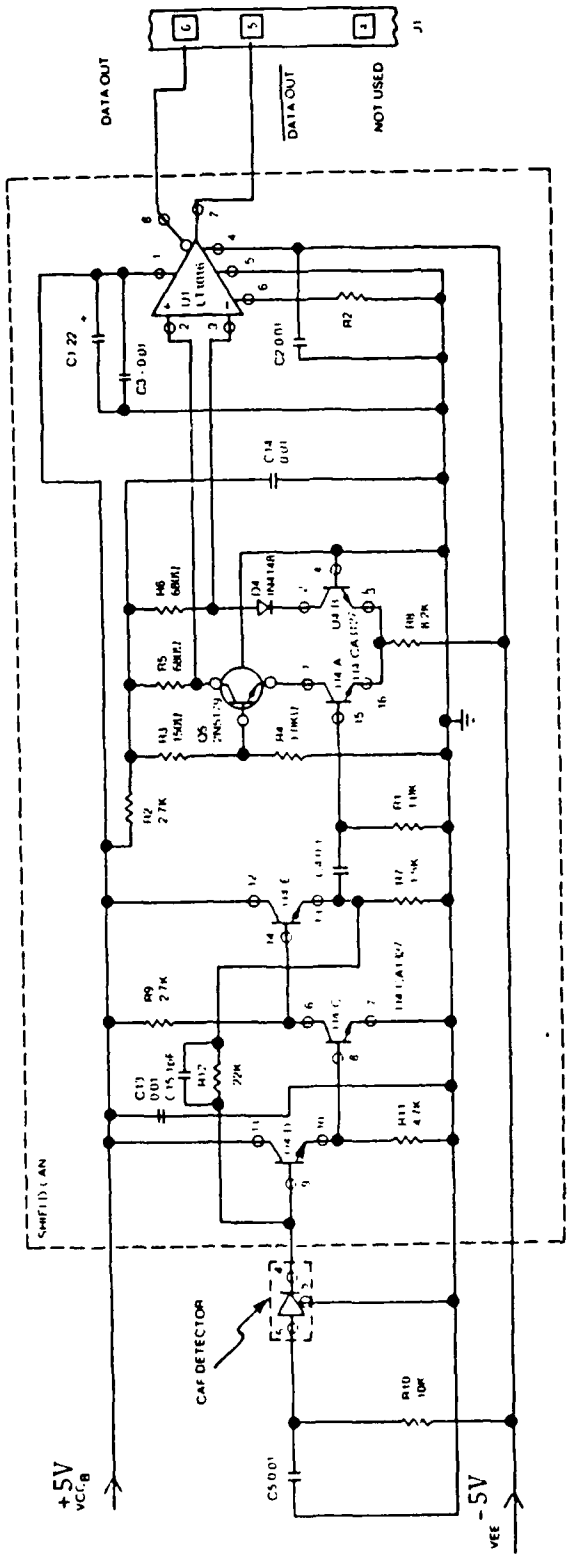


Figure 21a. CAF Receiver Circuit
[from Ref. 1:p. 7]

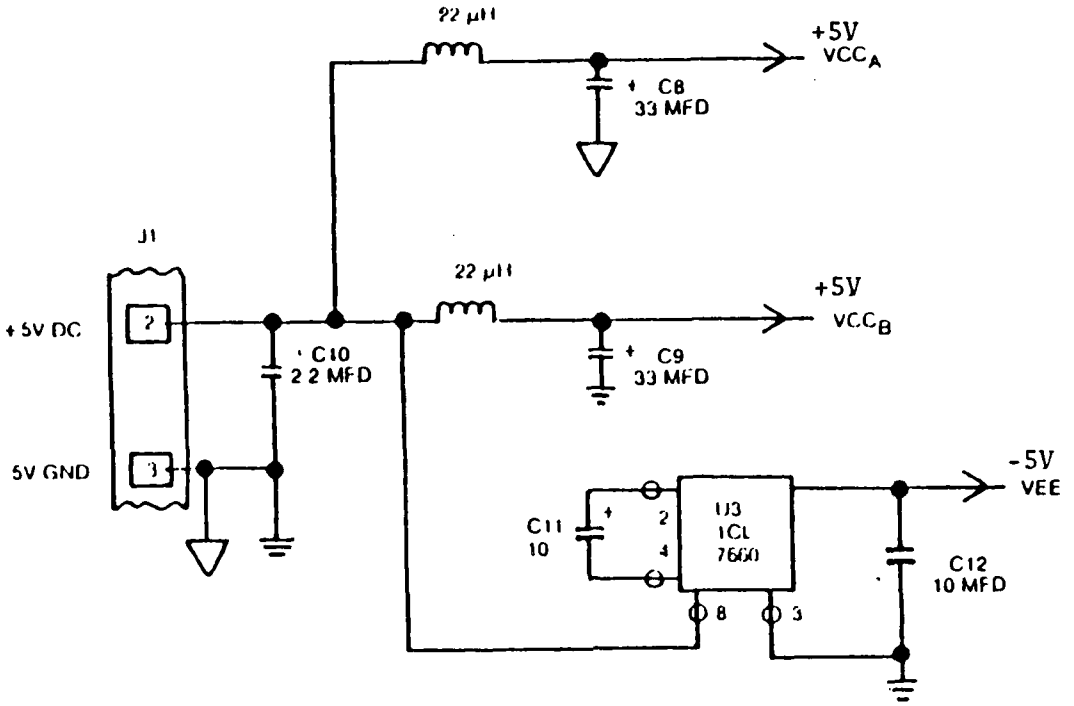


Figure 21b. -5v Rail Generator for CAF
[from Ref. 1:p. 7]

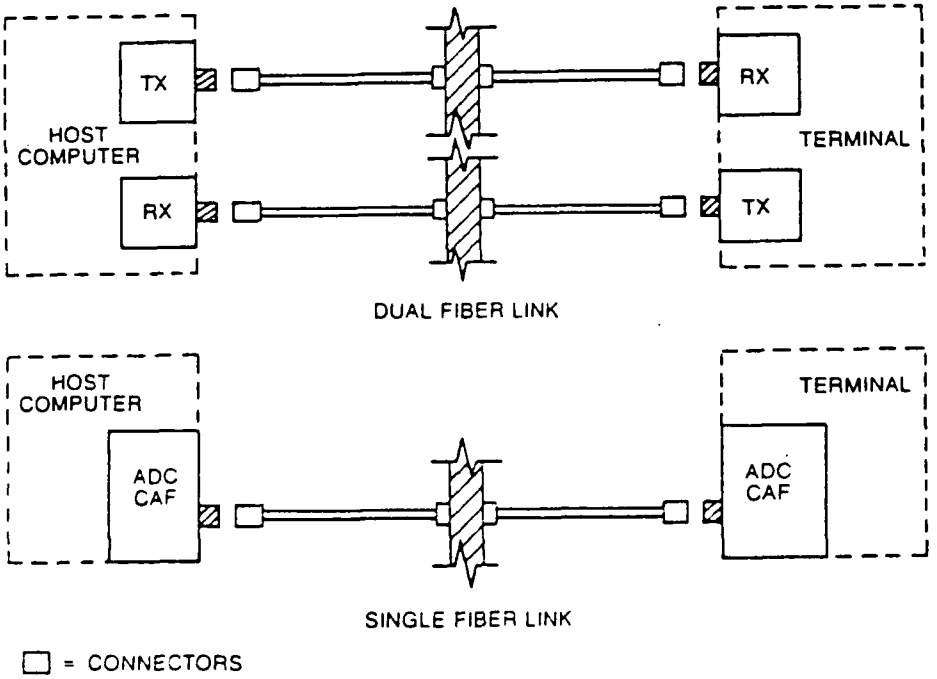


Figure 22. Example of F/O Line Reduction
Achieved by Using a Pair of CAFs
[from Ref. 1:p.14]

The CAF was chosen for transmission/reception of data signals for this project due to its wavelength division multiplexing (WDM) feature. WDM as it applies to this research is described in section E of this chapter.

2. A receiver/transmitter pair, the HFBR 2402/HFBR 1402 from the Hewlett-Packard HFBR-0400 series, was chosen for the transmission/reception of the control signals after conversion to optical signals. These components are readily available, they are very versatile in terms of size of fiber with which they are compatible and their interface electronics are relatively simple. Cutaway views of the HFBR 1402 and HFBR 2402 are shown in Figures 23a and 23b.

The transmitter has a typical response time of approximately 4.0 ns. This response time is more than adequate for transmission at 19.2 kilobaud as required for this thesis. The HFBR 1402 requires a drive circuit, as shown in Figure 24. The circuit of Figure 24 changes TTL level signals to optical signals.

The receiver, HFBR-2402, is essentially a photodetector and a DC amplifier. The circuit of Figure 25 converts received optical signals to TTL signals. The receiver is rated for up to 5 Mbaud data link design [Ref. 2]. The HFBR 2402 provides an inverted version of the transmitted TTL data after reconversion of the received optical signal to a TTL signal. This requires a compensating inversion in the electrical transmission path.

A more detailed description of this receiver/transmitter pair is provided in Reference 2.

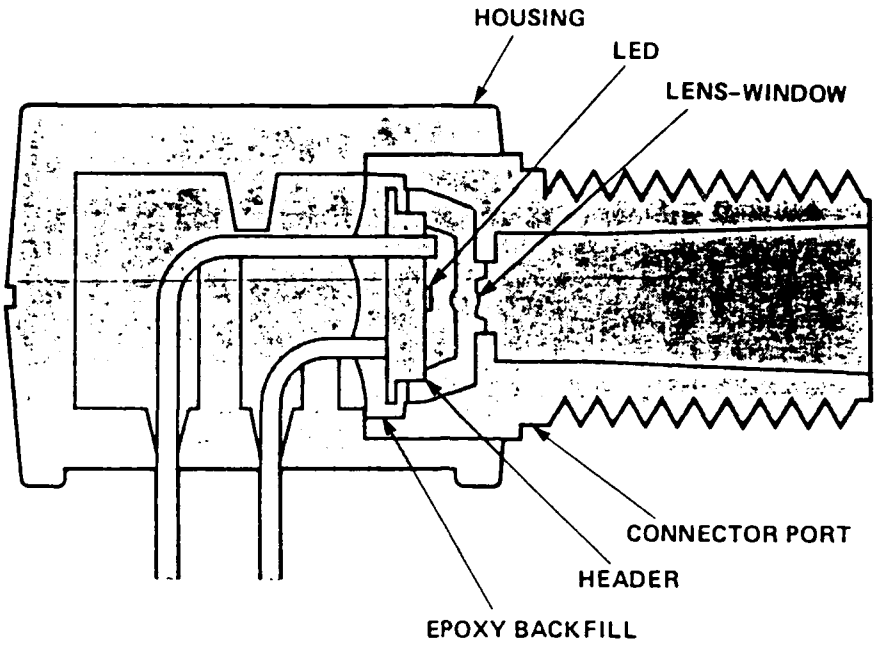


Figure 23a. HFBR 1402 Sectional View
[from Ref. 2:p.2]

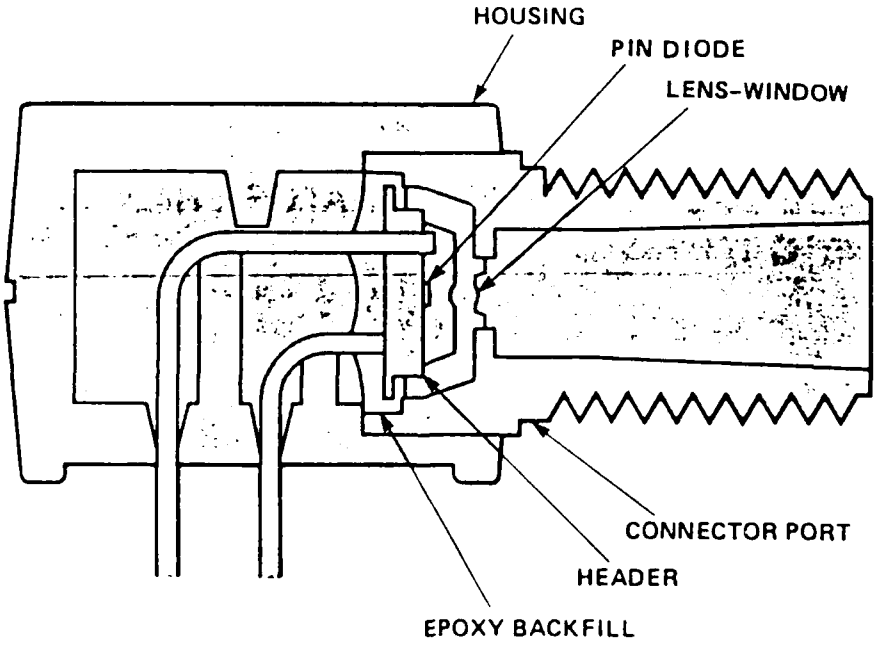


Figure 23b. HFBR 2402 Sectional View
[from Ref. 2:p. 6]

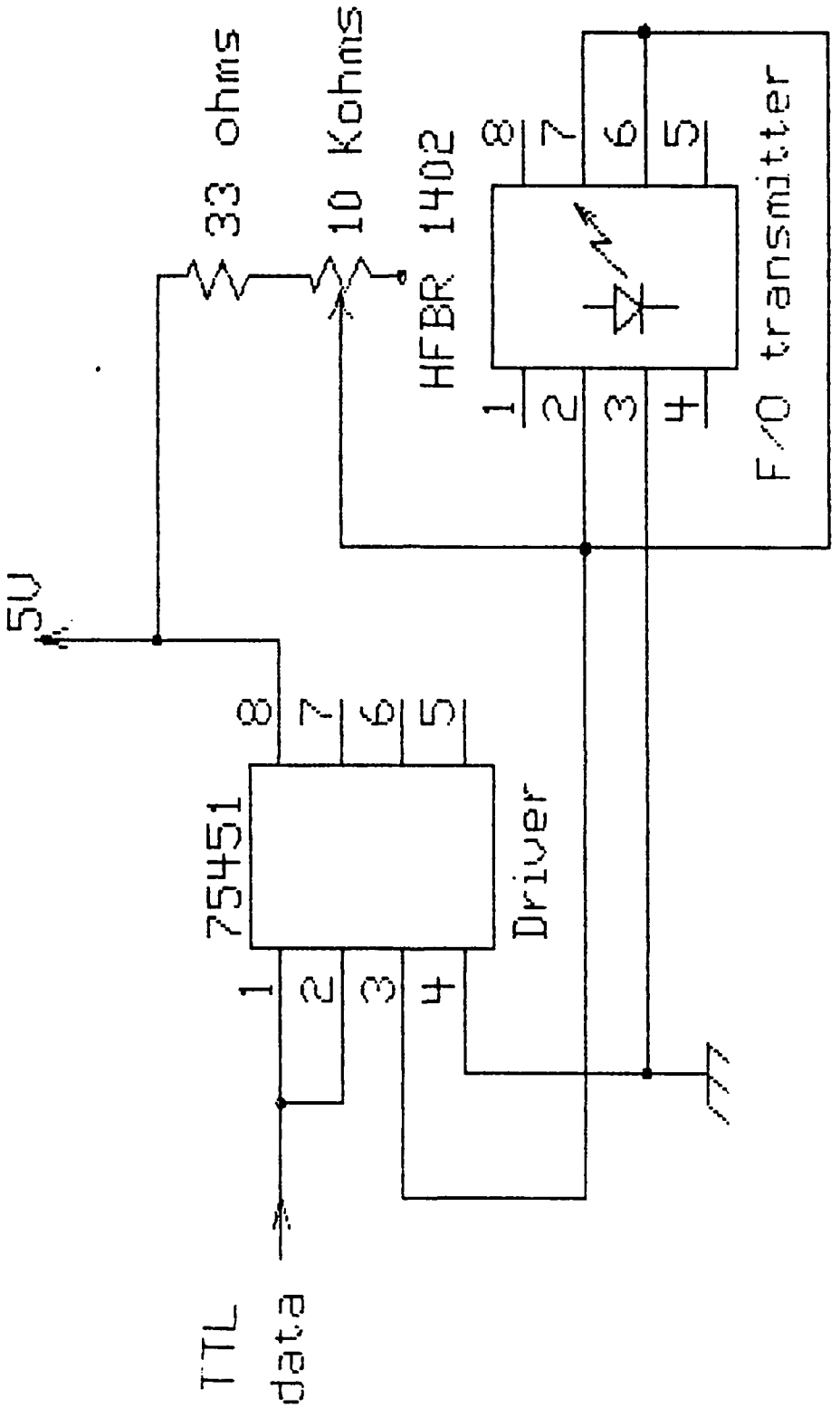


Figure 24. HFBR 1402 Drive Circuit
[Ref. 2:p. 5]

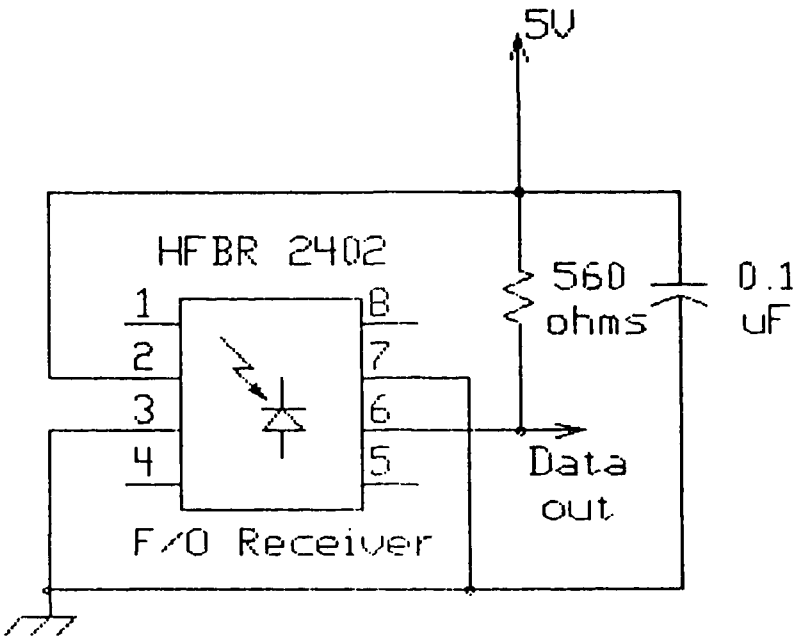


Figure 25. HFBR 2402 Receiver Circuit

3. The fiber chosen for use in this thesis is 100/140 um multimode fiber. The large core was chosen for coupling efficiency, ease of connectorization and ease of fusion splicing.

4. CANSTAR MC3-C-100 F/O T-couplers are used to combine and separate the transmit and receive optical wavelengths for the control signals to reduce the number of fibers from 3 to 2 for the final configuration (Figure 18). Data provided by CANSTAR QA division gives the measured insertion loss as less than 4 dB at each port. A photograph and a schematic diagram

of the CANSTAR T-coupler are provided in Figures 26a and 26b. Use of these F/O couplers to fabricate a fiber optic duplexer is described in the following section.

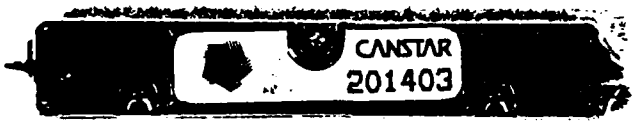


Figure 26a. CANSTAR T-Coupler

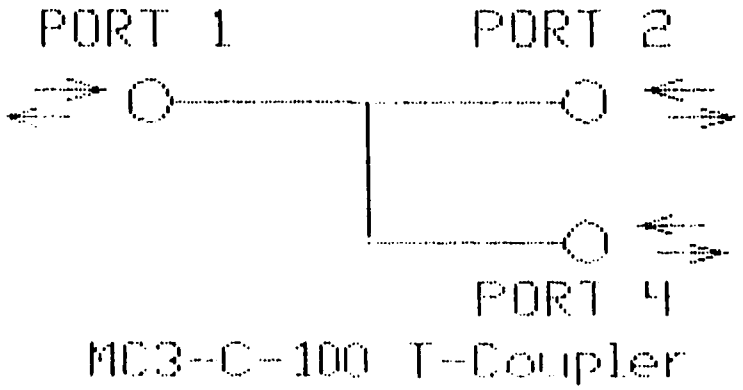


Figure 26b. T-Coupler Schematic

E. WAVELENGTH DIVISION MULTIPLEXING

The use of wavelength division multiplexing (WDM) and optical duplexing to reduce the number of fiber optic lines from four to two is described in this section.

WDM is the transmission and reception of two (or more) different wavelengths of light over the same optical fiber [Ref. 12:p. 188]. This technique allows more efficient usage of the enormous bandwidth of optical fibers and reduces the number of fibers required for any given interconnect. There are several methods by which optical wavelengths can be combined/separated to enable single fiber transmission/ reception. These include use of angular dispersion multiplexers/demultiplexers, such as prisms and diffraction gratings, and use of dichroic or interference filters [Ref.13:p. 4].

The ADC CAF, which was used to transmit and receive data signals over a single fiber, uses a dichroic filter technique. A dichroic filter is an optical filter which is constructed to transmit a specific frequency of light while reflecting another specific frequency [Ref. 1]. Here the word dichroic is used literally (meaning two-colored) [Ref. 14:p. 313]. (Note: the term dichroic is used more commonly in electro-optics to define the property of a material which absorbs one of the two orthogonally polarized components of incident light [Ref. 15:p. 89].)

A pair of CAFs accomplish bi-directional, full duplex optical transceiving in the following manner. Light emitted at 730nm from the source in CAF-01 in Figure 27 is transmitted by the Short Wave Pass (SWP) filter and focused into the fiber. At the distant end it is reflected by the Long Wave Pass (LWP) filter in CAF-02 and received by the photodetector. Light emitted from the source in CAF-02 at 865nm follows the reverse path [Ref. 1].

Optical duplexing is the coupling of optical carriers of the same wavelength but transmitted in different directions into the same fiber. This technique is used to reduce the number of fibers required to transmit and receive the multiplexed control signals from two to one.

Two of the CANSTAR T-couplers, previously described, were used to fabricate the fiber optic duplexer shown schematically in Figure 28. The optical signal coupled into port 1 is transmitted to port 3 and to port 4. At port 3 is a transmitter which does not react to incoming light. At port 4 the transmitted signal arrives at a receiver. The coupler exhibits insertion loss due to the splitting of the signal which must be taken into account when doing the link power budget analysis in Chapter VI. The optical signal at port 1 does not cause a signal to appear at port 2. Similarily, optical signals coupled into port 3 are received at port 2 and ignored at port 1.

Both signals are transmitted by HFBR sources at 820nm. The connectors are Subminiature Type-A (SMA) connectors compatible with the optical transmitters and receivers. All splices are fusion splices made with the Orionics FW-301 fusion splicer. The optical duplexer allows duplex optical transmission and reception of the multiplexed RS-232 control signals.

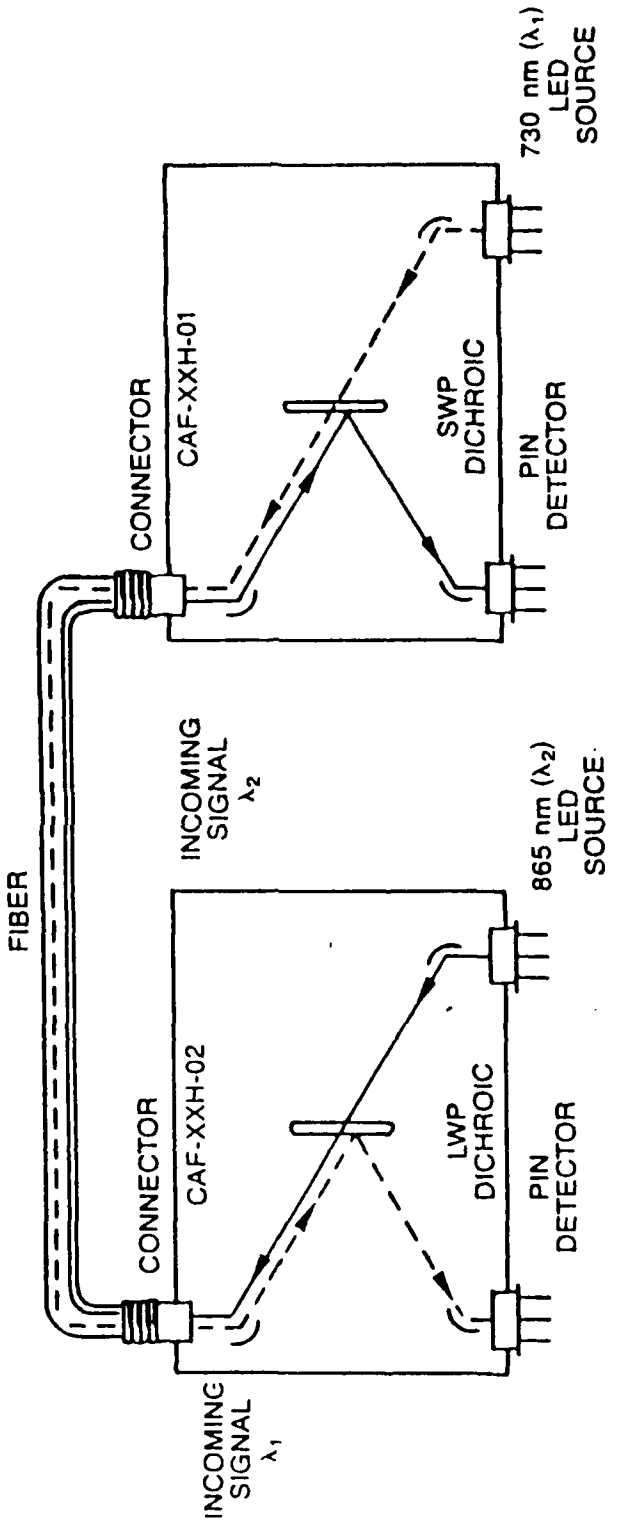


Figure 27. WDM Operation of CAF
[from Ref. 1:p. 5]

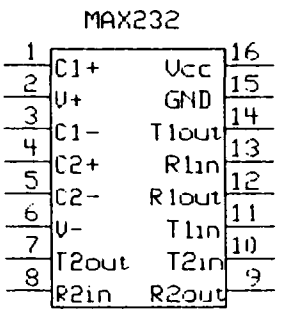
Figure 28. F/O Duplexer

III. DESIGN

This chapter contains design specifics for the major building blocks of the circuit. These include the RS-232-to-TTL conversion, the multiplexing and demultiplexing of the control signals and the pleisiochronous interface between transmit and receive sides of the circuit.

A. RS-232-TO-TTL AND TTL-TO-RS-232 CONVERSION

The MAX 232 chips employed in this thesis contain four level translators, two of which convert RS-232 signals to TTL signals and two of which perform the reverse operation. As opposed to more conventional conversion schemes which require split rail power supplies (typically +/-12v) for TTL-to-RS-232 signal conversion, the MAX 232 chip uses a single +5v power source to generate the +/-10v power supplies using charge pump voltage converters. [Ref. 16] The pin connections for the MAX 232 chip are shown in Figure 29a and a typical configuration for a four input/output application is depicted in Figure 29b.



IMPORTANT NOTE

Pin 8, labled R2in, is an RS232 input Pin 9, labled R2out, is the corresponding TTL output Pin 10, labled T1in is a TTL input Pin 7, T1out, is the corresponding RS-232 output

The other I/O pairs are also labled in this fashion

Figure 29a. MAX 232 Pin Connections [from Ref. 16:p. 1]

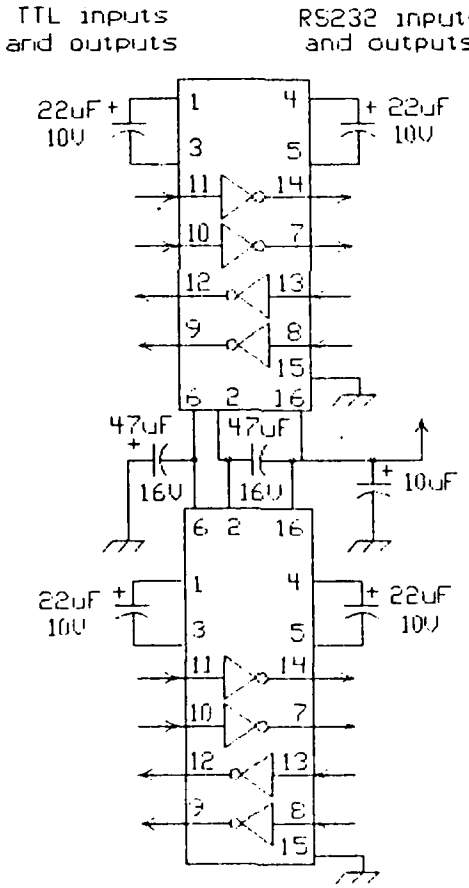


Figure 29b. MAX 232 Application [Ref. 16:p. 1]

It is important to note the inversion present in each conversion path. The input/output pairs are given in the following table:

TABLE 4
MAX 232 INPUT/OUTPUT PIN FUNCTIONS
[from Ref. 16:p. 1]

PIN #	FUNCTION	PIN #	FUNCTION
8	RS-232 INPUT	9	TTL OUTPUT
13	RS-232 INPUT	12	TTL OUTPUT
11	TTL INPUT	14	RS-232 OUTPUT
10	TTL INPUT	7	RS-232 OUTPUT

B. MULTIPLEXING AND DEMULTIPLEXING CONTROL SIGNALS

The method used for multiplexing and demultiplexing the control signals for the interface is Time Division Multiplexing (TDM). The two RS-232 control signals used for the null modem interface (after conversion to TTL levels) are sampled in turn and transmitted sequentially using a 74LS153 Dual 4-Input Multiplexer. The signal on one of the four input pins is selected by the address on the select pins of the multiplexer and is transmitted to the output pin. The reason for providing four channels to send two signals was to allow for future expansion. The chip pin connections and truth table are shown in Figures 30a and 30b.

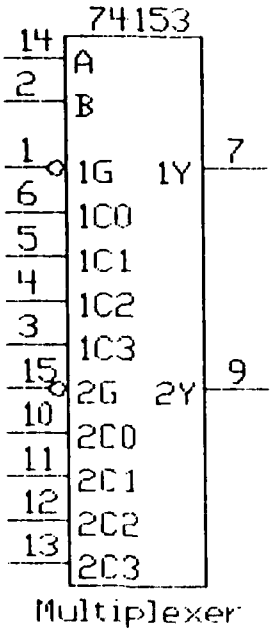


Figure 30a. 74LS153 Pin Connections [from Ref. 17:p. 2-465]

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Figure 30b. 74LS153 Function Table [from Ref. 17:p. 2-465]

The demultiplexing process is a reversal of the multiplexing process. It employs a 74LS155, Dual one-to-four Line Demultiplexer. The pin connections for the demultiplexer are shown in Figure 31a and the truth table is given in Figure 31b.

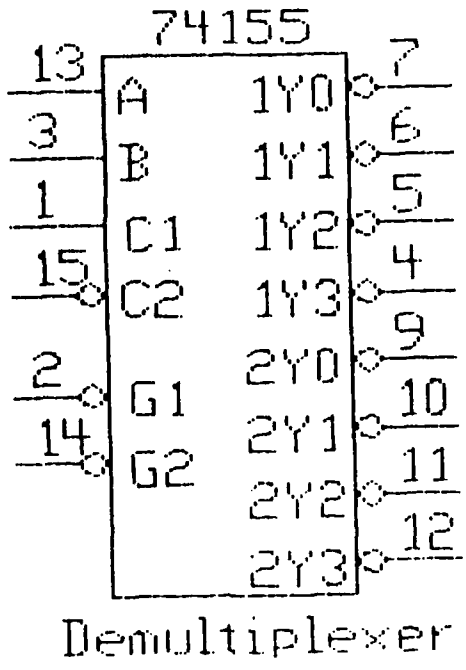


Figure 31a. 74LS155 Pin Connections
[from Ref. 17:p. 2-475]

Inputs				Outputs			
Select		Strobe	Data				
B	A	$\overline{G2}$	$\overline{C2}$	$\overline{2Y0}$	$\overline{2Y1}$	$\overline{2Y2}$	$\overline{2Y3}$
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H
B	A	$\overline{G1}$	C1	$\overline{1Y0}$	$\overline{1Y1}$	$\overline{1Y2}$	$\overline{1Y3}$
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Figure 31b. 74LS155 Function Table
[from Ref. 17:p. 2-475]

Notable features of the demultiplexer are that data arriving on input pin C2 is true at the selected output pin, while data at C1 is inverted at the selected output. All the output pins are high unless selected, at which time they either follow or invert the input as stated above.

The select lines of the multiplexer are driven by the QC and QD outputs (shown in Figure 32a) from a 74LS163 Synchronous Binary Counter with Synchronous Clear. This counter is clocked by a 1 MHz crystal oscillator. The counter was clocked at 1 MHz so that a mark or space data signal at 19.2 kilobaud would be three times the period of the counter cycle. This insures that the counters can complete their cycle and be cleared during one data bit time. With the circuit described in the next section, this allows nearly synchronous starting of the multiplexing and demultiplexing of the control lines during data transfer. The "ripple carry out" output of the counter is used as described in the following section. The select inputs for the demultiplexer are driven by a separate but similar counter and crystal oscillator circuit. The pin connections for the counter and its truth table are shown in Figures 32a and 32b.

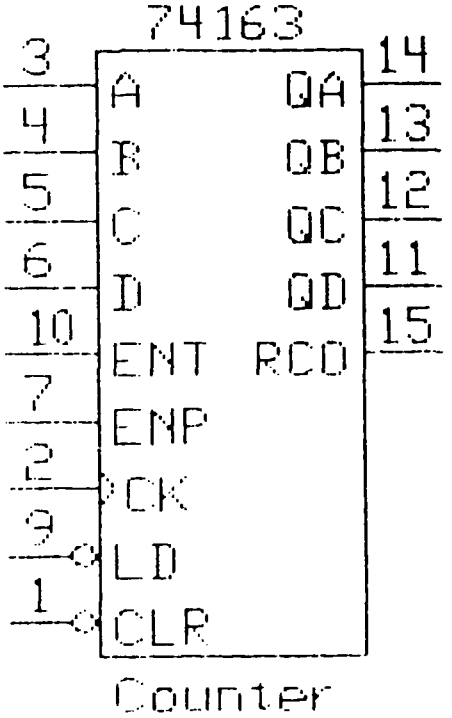


Figure 32a. 74LS163 Pin Connections
[from Ref. 17:p. 2-493]

CLK	$\overline{CLR}$	ENP	ENT	$\overline{LD}$	Function
↑	L	X	X	X	Clear
X	H	H	L	H	Count/RC Disable
X	H	L	H	H	Count Disable
X	H	L	L	H	Count/RC Disable
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Cntr

Figure 32b. 74LS163 Function Table
[from Ref. 17:p. 2-493]

For the null modem interface described previously, it is necessary to multiplex the two outgoing control signals Request to Send and Data Terminal Ready, transmit and receive these signals and demultiplex them and route them to the control inputs Clear to Send and Data Set Ready, respectively. Figure 33 depicts the multiplexing/ demultiplexing concept showing only the multiplexer, demultiplexer, counter and oscillator chips.

In the circuit shown in Figure 33, the clocks and the counters are considered to be synchronized so that the waveforms on the input select lines match the waveforms on the output select lines. In the following section the actual implementation of this synchronization is described. The circuit of Figure 33 also omits conversion to and from optical levels and shows a direct connection from the output of the multiplexer to the input of the demultiplexer. The conversion to and from optical levels inverts the signal arriving at the demultiplexer. Consequently, the actual implementation has an inverter in series with each demultiplexer output.

Figure 33 shows four multiplexer and four demultiplexer channels used to multiplex and demultiplex two control signals. This allows future expansion of the control signal multiplexing and demultiplexing to four channels in each direction without a major redesign effort.

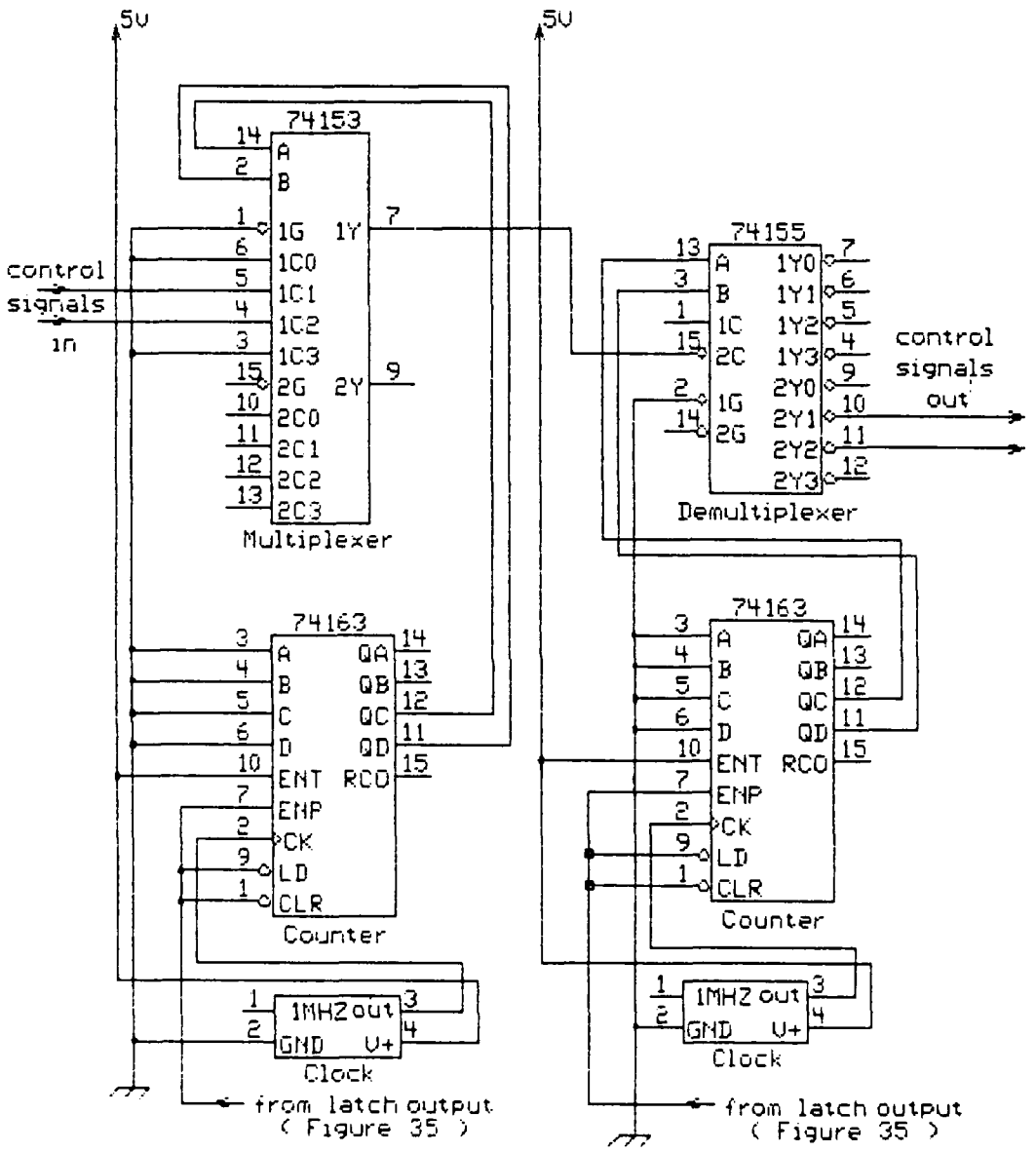


Figure 33. Multiplex/Demultiplex Configuration

C. PLEISIOCHRONOUS INTERFACE

The organization of the following two sections is derived from notes provided by Professor F. Terman of the Naval Postgraduate School. Portions of the text in sections C and D are paraphrased from those notes.

As was stated in the previous section, the multiplex inputs and the demultiplex outputs must be selected at the same rate and in the same sequence in order to insure that the handshaking signals are routed to the proper destinations. One common technique for recovery of the clock at the receiver is Manchester encoding or self-clocking code. In this technique a logic transition in the middle of each bit period is used to encode both clock and data within the same bit stream. The direction of the transition represents the data and the existence of the transition provides the clock rate for recovery at the receiver. [Ref. 18:p. 7] Implementation of a Manchester encoding scheme was not pursued for this thesis research due to its complexity.

The implemented approach is a pleisiochronous interface, where pleisiochronous is defined as "nearly synchronous". This means that each clock in the network (in this case each of the two clocks) is independent but relatively accurate. The system timing must be periodically readjusted due to the relative drift of the clocks to maintain the "nearly synchronous" condition [Ref. 19:p. 284-5].

In order to implement such a system for this thesis, a method was required to start the multiplexing and demultiplexing operations almost simultaneously. A way to reset the counters when the required sequence of select signals had been produced was also required. The interface designed for this thesis uses two 1 MHz crystal oscillators to clock two separate counters which in turn control the multiplexing and demultiplexing operations. Each multiplexer/demultiplexer cycle is 16 clock pulses (16 us) in length. These cycles are divided into four time slots of 4 us each. During each time slot one of the four control channels is transmitted over the fiber optic link.

Nearly synchronous operation occurs when each demultiplexer cycle begins within one clock pulse of the corresponding multiplexer cycle. Once the multiplexer/demultiplexer cycles are synchronized, the oscillators are stable enough to insure synchronization for approximately one second with the counters running continuously. Each multiplexer/demultiplexer cycle should be allowed to complete normally before resynchronization. Specifically, resynchronization should take place between multiplexer/demultiplexer cycles.

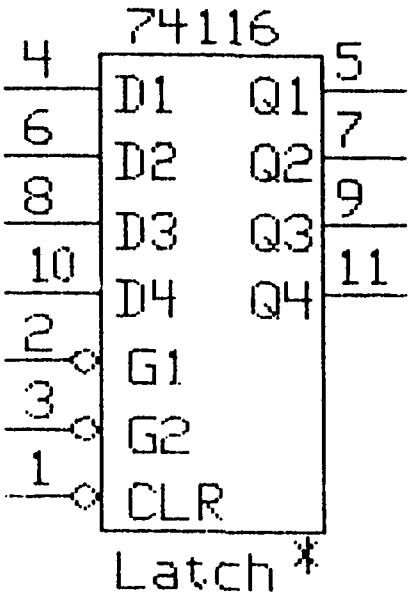
Two 74LS116 D-latches are used to start and stop the counters to insure that the multiplexer/demultiplexer cycles are not interrupted. These latches are also used to maintain effective synchronization of the multiplexer/demultiplexer

cycles. The pin connections and the truth table for the 74LS116 Dual 4-Bit Latches with Clear used for this purpose are shown in Figures 34a and 34b. The wiring diagram for the latch and counter implementation is shown in Figure 35. Connections previously shown in Figure 33 are omitted in Figure 35.

The multiplexer counter is enabled when the latch output is high. The counter is cleared synchronously when the latch output is low. The output waveforms on QC and QD of the counter are used to select the multiplxer input channel. The demultiplexer side of Figure 35 operates in a similar manner.

The outputs of the latches in Figures 35 are fed back to one of the active low enable inputs of the latch. When the latch output is low, the latch is transparent and the output follows the input. When the latch input goes high, the output goes high. The high ouput signal fed back to the active low enable input disables the latch. The latch essentially "catches" the high output. The latch output can now only be brought low by presenting a low signal to the active low clear input of the latch.

Each counter in Figure 35 will be held clear when stopped if a low signal is on the input to its respective latch. Applying a high signal at the input to either latch will start the associated counter. Fifteen clock pulses after counting begins, the Ripple Carry Out (RCO) output of the



* For the dual quad latch pins 13-23 have the same functions as pins 1-11

Figure 34a. 74LS116 Pin Connections
[from Ref. 17:p. 2-357]

Inputs				Output
$\overline{CLR}$	Enable		any D_i	any Q_i
	$\overline{G1}$	$\overline{G2}$		
H	L	L	L	L
H	L	L	H	H
H	X	H	X	Q_0
H	H	X	X	Q_0
L	X	X	X	L

Figure 34b. 74LS116 Function Table
[from Ref. 17:p. 2-357]

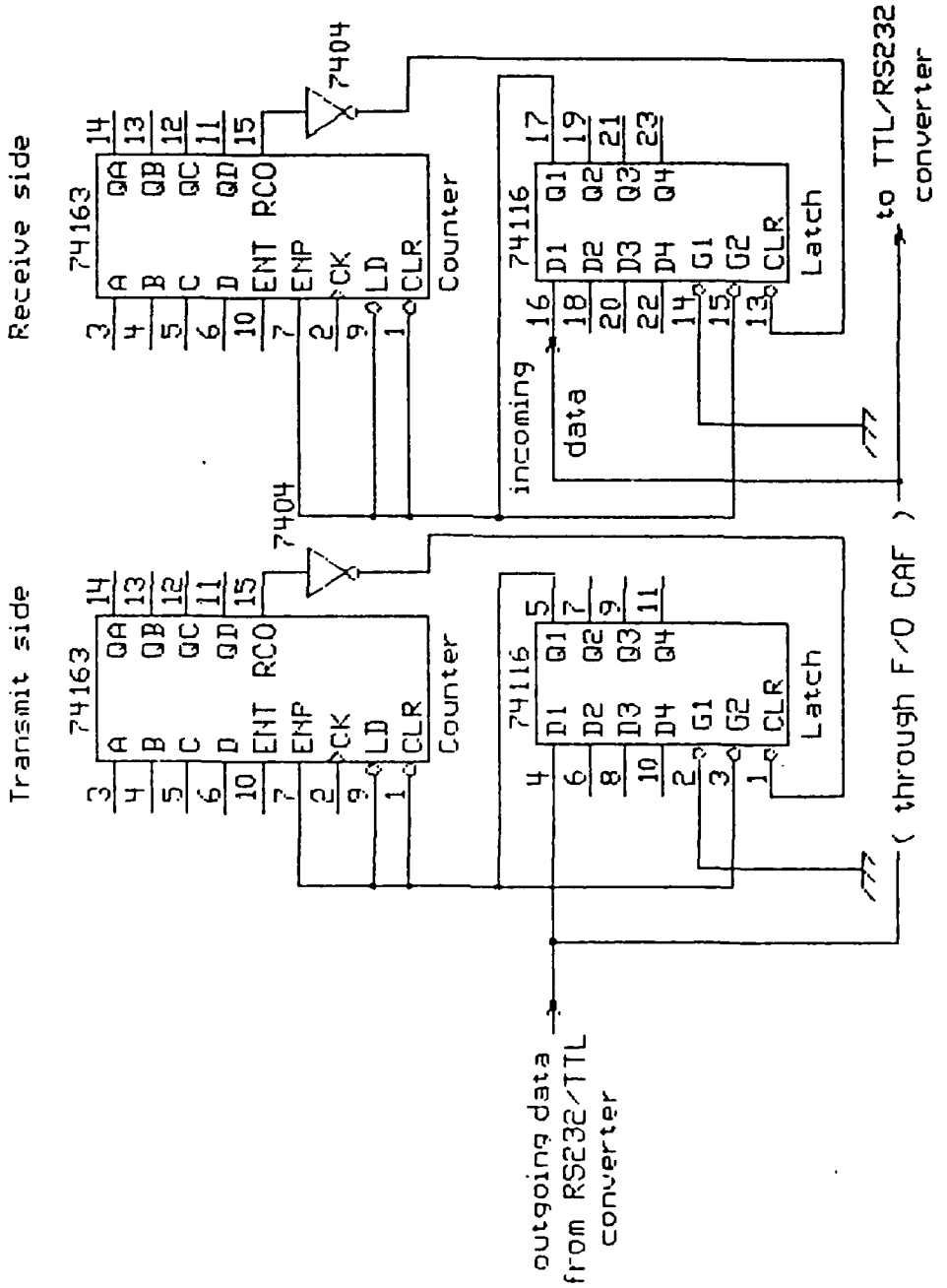


Figure 35. Latch and Counter Implementation

counter will go high. The inverted RCO output will clear the controlling latch. The 16th clock pulse will clear the counter. If the latch input is still high, the latch output will follow once the RCO goes low. In this case, the counter will resume counting and the cycle will repeat. If the input to the latch is low when the counter is cleared, the output will stay low and the counter will be held stopped and cleared.

The latch and counter arrangement of Figure 35 is used to maintain the effective synchronization of the multiplexer counter and the demultiplexer counter during data transmission. The inputs of both latches are connected to the TTL level data line and the mark and space data bits are used to synchronize the two counters. When an RS-232 space (+9V) bit, is followed by an RS-232 mark (-9V) bit, synchronization occurs. Since each data frame begins with a space (the start bit) and ends with a mark (the stop bit), resynchronization will take place at least once for each data frame.

A space data bit, after conversion and inversion by the MAX 232 to TTL logical 0 voltage level, will drive the mutliplexer latch input low. At the interface data rate of 19.2 kilobaud, this low signal will persist for 52 us. Since this is more than three times longer than the full cycle of the multiplexer counter, the counter will complete its cycle

and be cleared and disabled. When the next mark data bit is transmitted, the leading edge of the mark bit (at TTL logical 1 level) will be caught by the latch. The high output of the latch will enable the counter which will begin to count on the rising edge of the next clock pulse from its oscillator.

The same space data bit will be received at the distance end and will clear and disable the demultiplexer counter when the current counter cycle is complete. The same mark data bit which started the multiplexer counter will be latched by the demultiplexer latch and will start the multiplexer counter on the rising edge of the next clock pulse from its oscillator. The two counters will be nearly sychronized since they will have started within one clock pulse (1 us) of each other.

Phase "glitches" (1 us long at most) will result from the imprecise starting of the two counters. During the first or last microsecond of a time slot, the control signal from an adjacent channel may appear on the selected demultiplexer output channel. These phase "glitches" will not be converted into RS-232 levels signals by the MAX 232 due to its relatively slow output risetime. A method for eliminating the phase "glitches" entirely is proposed in Chapter VI.

The end-to-end circuit design is described in the following section. The discussion also addresses the time intervals in which data is not being transmitted. The following section also explains why a sample and hold on the

output of the demultiplexer channels is not required for proper operation of the HP-150-to-HP-150 interface.

D. OVERALL CIRCUIT DESIGN

The complete circuit diagram of one side of the interface is shown in Figure 36. The distant end of the interface is identical. The two ends of the interface are connected through fiber optic links as previously shown in Figure 18. Connections between individual circuit elements are based on the functions previously discussed and the pin connections and truth tables previously provided.

At this point, a discussion of how data transfer between the two HP-150s is enabled or inhibited is necessary. The HP-150s were observed to require continuously asserted signals on both the Clear to Send (CTS) and the Data Set Ready (DSR) control inputs of the transmitting HP-150 to enable data transfer. The HP-150s were also observed to halt data transmission when a negated control signal (-9V) was detected, even briefly, on either the CTS or the DSR input. Once halted, data transmission did not resume until a continuously asserted control signal was presented at the control inputs of the transmitting HP-150. The end-to-end circuit design was developed to accommodate these HP-150 characteristics for both synchronized multiplexing and demultiplexing and unsychronized multiplexing and demultiplexing.

The following paragraphs explain both the synchronized and unsynchronized operation of the interface circuit for both asserted and negated control signals. The synchronous operation of the circuit is discussed first. A discussion of non-synchronous operation follows the synchronous discussion.

When data is being transmitted, the multiplexer counter and the demultiplexer counter are synchronized. In this case, an asserted signal on a particular control input is required to give an asserted output on the corresponding control channel at the demultiplexer.

As can be seen from Figure 36, the two unused control channels of the multiplexer have grounded inputs. These connections were made so that all four input channels to the multiplexer would be asserted when the active channels were asserted. A grounded input on the multiplexer represents an asserted control channel because the MAX-232 inverts the asserted (+9V) RS-232 control signal when converting it to a TTL-level signal. (Note: these grounded inputs are critical to the unsynchronized operation of the circuit.)

The driver and detector circuits for the HFBR 1402/2402 link used to transmit the muliplexed control signals produce a TTL-level received signal that is the inversion of the TTL-level transmitted signal. As a result, the inversion in the MAX 232 on the input side of the interface is cancelled. After demultiplexing, an asserted (+9V) RS-232 control input signal appears as a high TTL signal on the corresponding

demultiplexer output. The inversion in the MAX 232 at the output side of the interface is accommodated by inverting the output of each demultiplexer channel. As a result of the even number of inversions in the transmission path, an asserted control signal at the input side of the interface produces an asserted control signal at the output side of the interface. This result is valid during the time slot in which the particular control channel is selected at the demultiplexer.

Recall that the HP-150 requires a continuously asserted control signal on both the CTS and the DSR inputs. This means that the control inputs must remain asserted during the time slots in which their associated demultiplexer channel is not selected. As shown in Figure 31b, the output of any demultiplexer channel is high unless selected. When a channel is selected, its output follows the input to the demultiplexer. Thus, the output of an asserted control channel at the demultiplexer is high when selected and high by default when not selected. This results in a continuously asserted control signal at the output of the interface circuit. If both control channels at the input to the interface circuit are continuously asserted, then both control channels at the output of the interface circuit are asserted. Data transfer is enabled.

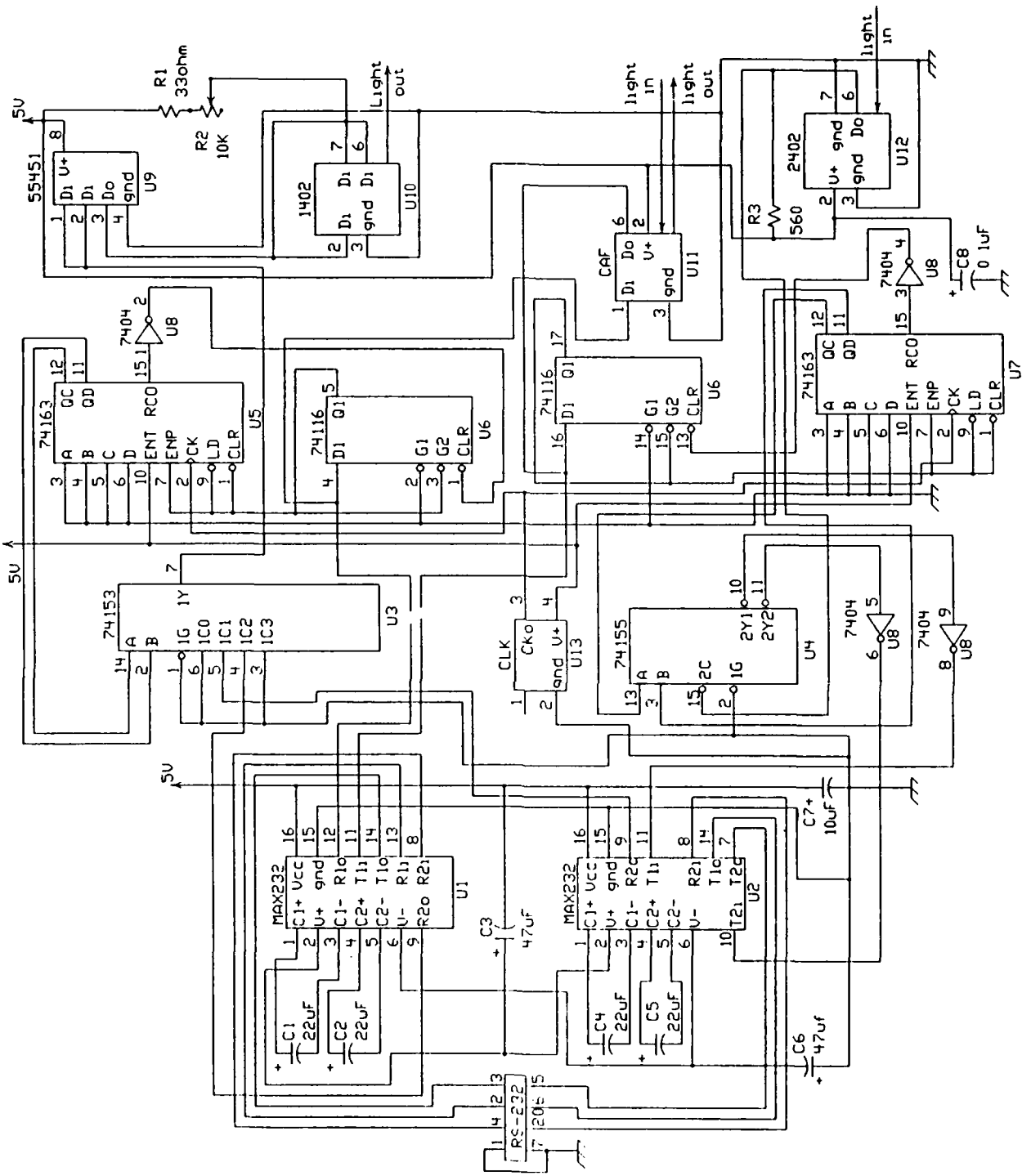


Figure 36. Complete Circuit Diagram
(Note:On chips with Vcc connections "on the corners", (e.g., pin 16 for Vcc, pin 8 for ground on a 16 pin chip) those connections have been suppressed. Non-standard Vcc and ground connections are shown.

The transmitting HP-150 will halt data transmission when a negated control signal (-9V) is detected even briefly on either its Clear to Send (CTS) or its Data Set Ready (DSR) input. When a particular control signal is negated at the input to the interface circuit, it is presented to its multiplexer input as a TTL-level high signal. After inversion in the HFBR 1402/2402 electro-optic link, it appears as a low signal at the appropriate demultiplexer output when that output is selected. In this case, the demultiplexer channel output is low when selected and high otherwise. This signal appears at the corresponding control output of the interface circuit as a periodically negated control signal. As previously stated, this periodically negated control signal inhibits data transfer. A more detailed description and oscilloscope pictures of the control waveforms are provided in Chapter IV.

When data is not being transmitted, an RS-232 data line is held at the mark level (-9V). After inversion by the MAX 232, this presents a logical 1 TTL level to both latches causing the counters to run continuously. Control signals are transmitted over the fiber link whenever the counters are running. As no data is being transmitted, resynchronization of the counters does not occur. The counters drift out of synchronization and the control signals appear periodically on the wrong channels at the distant HP-150. Due to the RS-232 interface characteristics and the design of the thesis

circuit, this lack of synchronization does not adversely affect operation of the HP-150-to-HP-150 data link.

For unsynchronized operation of the multiplexer and demultiplexer counters, continuously asserted control signals at the interface circuit outputs are still required to enable data transfer. This condition can be realized by grounding the unused input channels to the multiplexer. Grounded multiplexer inputs represent asserted RS-232 control signals due to the inversion in the MAX 232 at the input to the interface circuit.

In the unsynchronized condition, a particular input control signal appears on each demultiplexer output channel in sequence due to the relative drift between the multiplexer and demultiplexer counters. Since all of the multiplexer inputs are asserted when both control inputs to the interface circuit are asserted and the two unused control channels at the multiplexer are asserted, the outputs of the demultiplexer are all continuously asserted. This results in continuously asserted control outputs from the interface circuit to the transmitting HP-150, thereby enabling data transfer.

When the multiplexer and demultiplexer counters are unsynchronized, a negated signal on any of the input control channels to the interface circuit will produce a high signal in one of the multiplexer time slots. This signal will result in a periodically low signal at the input to the

demultiplexer. Due to the drift between the multiplexer and the demultiplexer counters, this low signal will appear on each demultiplexer output every few seconds. The control outputs from the interface circuit will thus be negated periodically. Period negation of either control input of the transmitting HP-150 (CTS or DSR) will inhibit data transfer.

Provision of a continuously negated control signal is therefore not required to inhibit data transmission. Chapter IV contains the results obtained from the test of the interface.

Due to the described characteristics of the HP-150 RS-232 interface, a sample and hold circuit for the demultiplexer channels during their selected time slots is not a design requirement. The interface circuit design described relies heavily on the properties of the HP-150 to operated properly. Several enhancements to the end-to-end design are proposed in Chapter VI. Those enhancements are intended to make operation of the interface independent of the properties of the terminal devices.

IV. ENGINEERING TEST AND EVALUATION

This chapter describes how the circuit building blocks were tested on a block-by-block basis and then on an integrated basis. Waveform in/waveform out comparisons are given for each major functional area.

A. TEST OF DATA TRANSMISSION/RECEPTION OVER CAF

The ADC CAFs were tested by applying a 20 kHz square wave with TTL electrical characteristics (+5V-to-0V) at one data input and observing the output on the distant CAF. The test was repeated for transmission in the opposite direction. The test resulted in accurate transmission of the test waveform in both directions.

B. TEST OF RS-232-TO-TTL (AND INVERSE) CONVERSION

To test the data and control signal format conversion from RS-232-to-TTL and back to RS-232, the circuit previously shown in Figure 29b was constructed using two MAX 232 chips. Signals with RS-232 electrical characteristics (+9V and -9V levels and a +/-9V square wave at 20 kHz) were applied to the RS-232 inputs and the corresponding TTL outputs were recorded. TTL signals (+5v and 0v dc levels and 5v pulses with 50% duty cycle) were applied to the TTL inputs and the corresponding RS-232 outputs were recorded. The results are shown in Table 5. Waveform in/waveform out comparisons for

the +/-9v square wave at 20 kHz and for the 5v pulse train at 40 kbps are shown in Figures 37a and 37b.

Testing of higher frequency waveforms showed that the highest data rate which could be accurately converted using this circuit was approximately 85 kHz. This 85 kHz square wave corresponds to a 170 kbps digital signal. Accurate conversion in this context means that conversion of a TTL pulse results in a square wave with RS-232 characteristics at the same data rate. This limiting data rate is important to the proper functioning of the interface. Recall that phase "glitches" were expected to appear on the demultiplexer output channels as described in Chapter III. Phase "glitches" approximately one clock pulse (1 us) wide were observed during testing. The MAX 232 TTL-to-RS-232 converter frequency response is too slow to convert a 1 us pulse into an RS-232 control signal. The phase "glitches" do not result in a significant change in the RS-232 signal level at the HP-150 and thus do not affect data transmission. More detailed information is provided in Chapter VI.

TABLE 5
RS-232-TO-TTL CONVERSION LEVELS

PIN #	INPUT SIGNAL	PIN #	OUTPUT SIGNAL
8 (RS-232 IN)	+9V -9V	9 (TTL OUT)	0V +5V
13 (RS-232 IN)	+9V -9V	12 (TTL OUT)	0V +5V
11 (TTL IN)	0V +5V	14 (RS-232 OUT)	+9V -9V
10 (TTL IN)	0V +5V	7 (RS-232 OUT)	+9V -9V

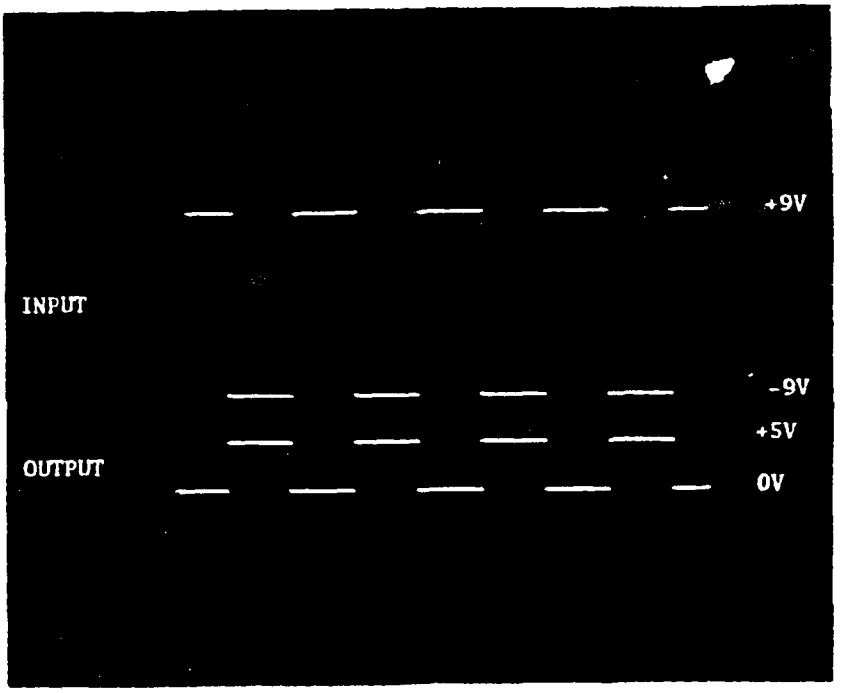


Figure 37a. RS-232-to-TTL Conversion

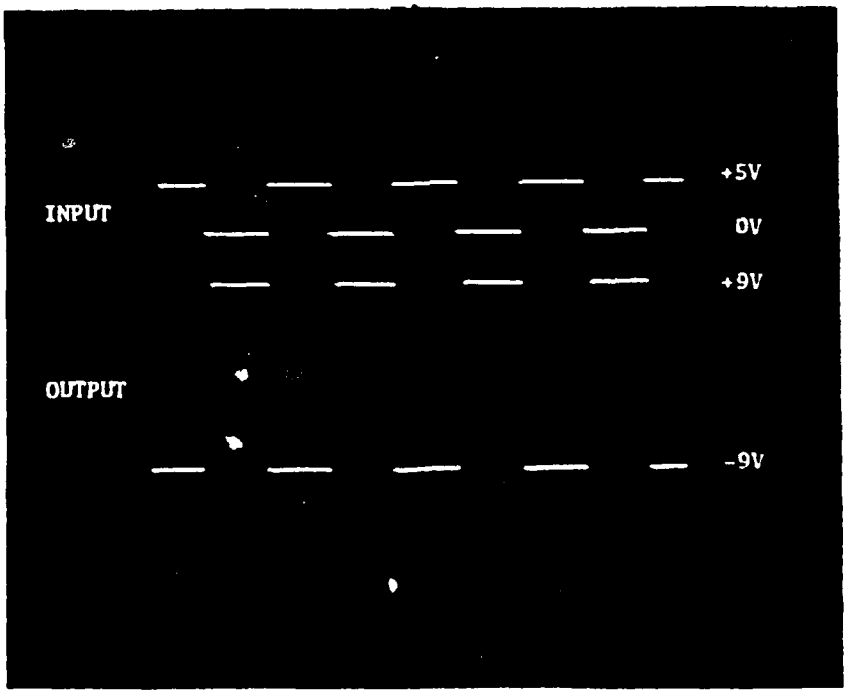


Figure 37b. TTL-to-RS-232 Conversion

C. TEST RESULTS OF MULTIPLEX AND DEMULTIPLEX OF CONTROL SIGNALS

The multiplexing of the control signals was tested by applying TTL-level control signals at the inputs of the multiplexer and recording the output waveforms. Demultiplexing was tested by applying the multiplexed control signal carrier directly to the input of the demultiplexer and recording the output waveform on each channel. This eliminates the inversion caused by the conversion to and from optical levels in the actual interface. For this test the same oscillator was used to clock both counters. One set of test control signals is depicted herein. The test control signals were constant level high and/or low RS-232 signals converted to TTL levels.

Recall that the output channels of the demultiplexer are at a high (logic 1) level, unless selected, at which time they follow their input. This presents a signal to the HP-150 that is not the same as the transmitted control signal. One combination of input control signals and the corresponding outputs are shown in Table 6. The multiplexed control signal carrier and one of the demultiplexed control channels are shown in Figure 38a and 38b for the combination of control signals shown in Table 6. Similar results were obtained for test of different control signal combinations. All four input/output channel pairs functioned properly.

As previously mentioned, in order to provide for future expansion, four multiplex/demultiplex channels are provided although only two control signals are multiplexed and demultiplexed.

TABLE 6
INPUT AND OUTPUT CONTROL SIGNALS AT MULTIPLEXER AND DEMULTIPLEXER CHANNELS

MULTI-PLEXER INPUT	INPUT CHANNEL	OUTPUT CHANNEL	DEMULTIPLEXER OUTPUT
+5V	1C0	2Y0	+5V
+5V	1C1	2Y1	+5V
0V	1C2	2Y2	+5V NOT SELECTED 0V WHEN SELECTED
+5V	1C3	2Y3	+5V

The three period high, one period low demultiplexer channel output is inverted by a 74LS04 as discussed in the following section. The signal is then re-inverted and converted to an RS-232 control signal by the MAX 232. The resulting control waveform is shown in Figure 38c. Although this "non-true" control waveform was sufficient to halt data transmission between the two HP-150s, it may not do so for other RS-232 interface devices. Two methods for restoration of true control signals from the demultiplexed output channel waveform are discussed in Chapter VI.

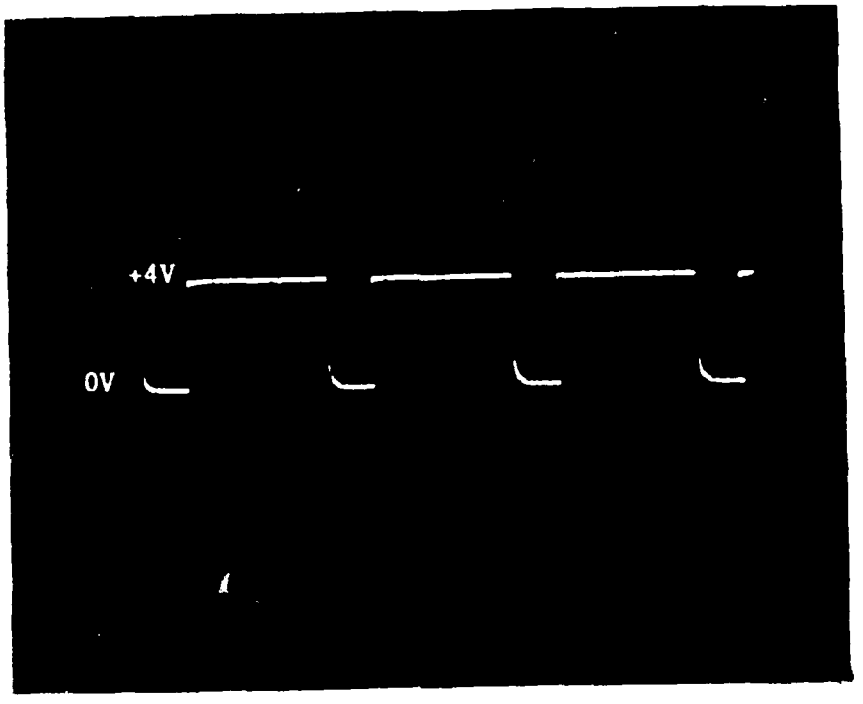


Figure 38a. Multiplexed Control Line Signal
(One low signal, three high signals)

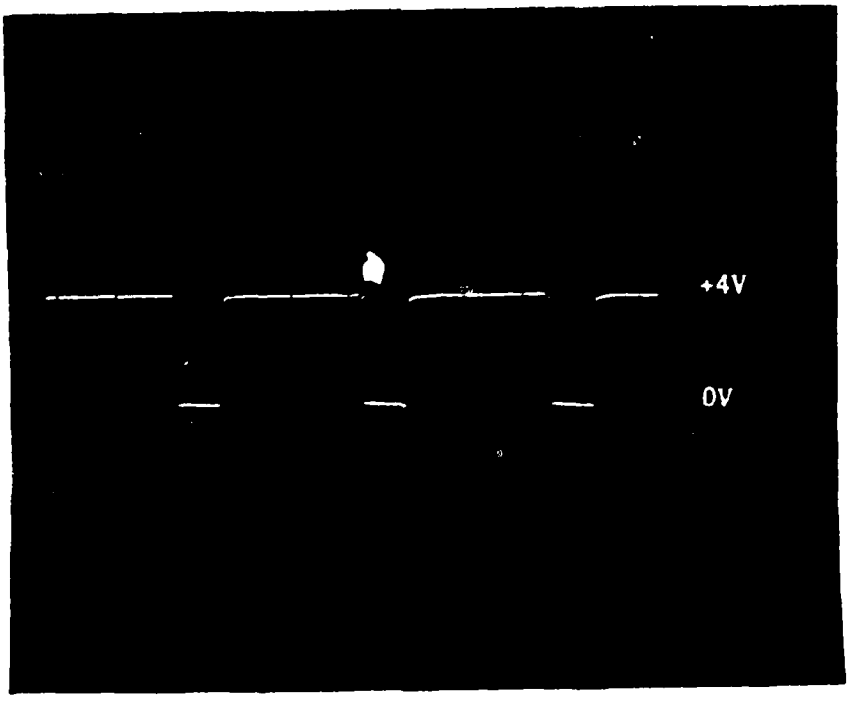


Figure 38b. Demultiplexed Control Channel
(High unless selected, then true to input)

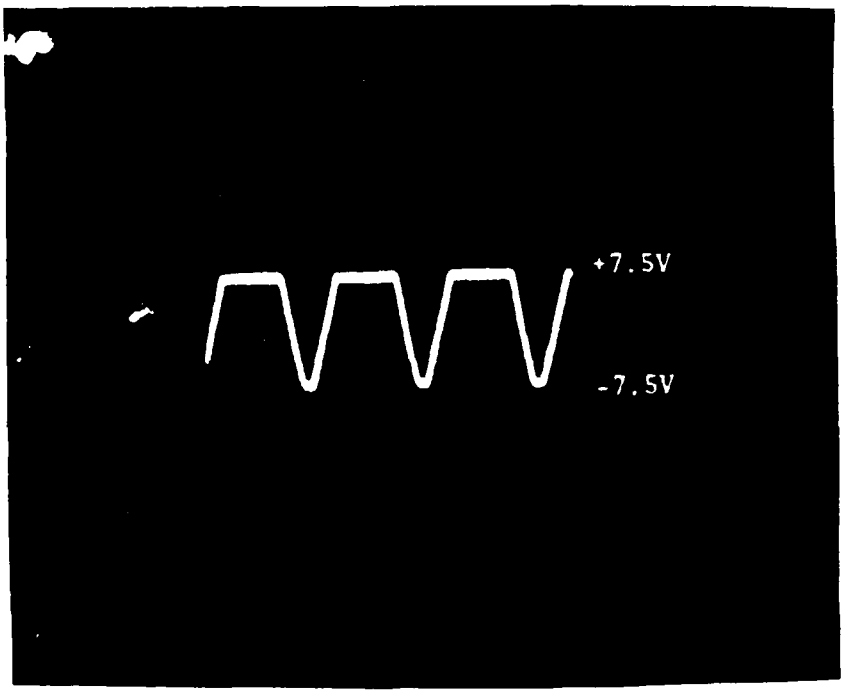


Figure 38c. Control Signal Presented to HP-150 When a Low Control Signal is Transmitted

D. TEST RESULTS OF CONVERSION OF MULTIPLEXED SIGNALS TO LIGHT FREQUENCY, TRANSMISSION/RECEPTION AND RECONVERSION TO TTL SIGNAL LEVELS

The TTL-level, multiplexed control signal bit stream was applied to the input of the HFBR 1402 F/O transmitter drive circuit (pins 1 and 2 of the 75451 Peripheral Driver previously shown in Figure 23). A length of 100/140 micrometer F/O cable was used to connect the HFBR 1402 and HFBR 2402. The output waveform was observed at pin 6 of the HFBR 2402 as shown (see Figure 24). The input and output waveforms are shown in Figure 39. Of particular interest is the signal level inversion from transmitter to receiver. This inversion is accommodated by introducing an inverter at the demultiplexer output (one inverter for each control signal).

Attempts to eliminate the inverters by using the C1 input to the demultiplexer were not successful. The output of the demultiplexer channel for a high RS-232 control signal was high unless selected, then low resulting from the inversion of the high control signal. When this output waveform was inverted by the MAX 232, the HP-150 received a waveform which halted data transfer. This was not the desired result for a high (+9V) control signal. As previously stated, when the control outputs are high, data transfer is supposed to be enabled.

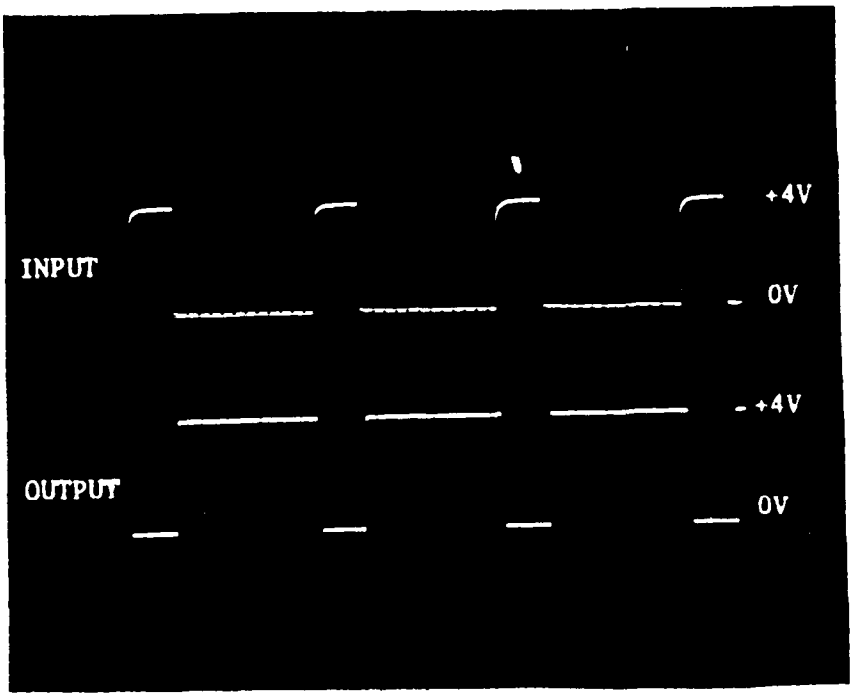


Figure 39. Input to HFBR 1402 Driver Circuit and Output from HFBR 2402

E. TEST OF FIBER OPTIC DUPLEXER

The F/O duplexer was fabricated as described in Chapter II and shown in Figure 28. It was tested using the Photodyne 7700XR Optical Signal Source and the Photodyne Model 22XLA Fiber Optic Multimeter. The test configuration is shown in Figure 40. An output reference level from the source of -26.5 dBm was established and applied at port 1. The output level at port 4 was measured and recorded as -32.9 dBm. The test was repeated for an input signal of -26.5 dBm at port 3 and the output level at port 2 was measured and recorded as -30.2 dBm. The significance of these power levels will be discussed in Chapter VI.

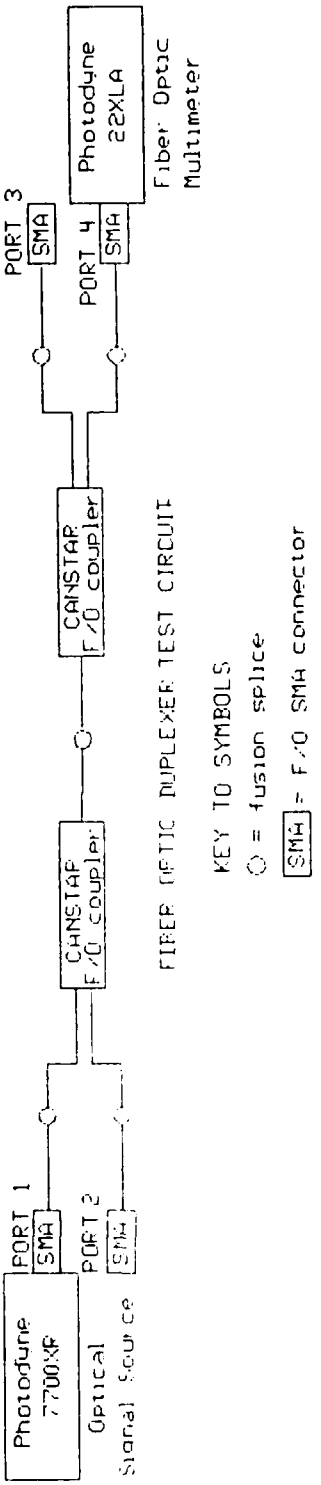


Figure 40. F/O Duplexer Test Configuration

F. TEST RESULTS FOR PLEISIOCHRONOUS INTERFACE

The counter and latch operation was tested using the circuit previously shown in Figure 35. The first objective was to observe the behavior of the circuit when the transmit data line was idle. An idle RS-232 data line sits at the mark (-9V) level giving a logical 1 (TTL level +5V) at the input to the latch. The input to the latch was initialized with a logical 0 for this test. When a logic 1 (TTL level +5V) was presented at the input to the latch (pin 4 or pin 16), the output went high. This high output was fed to one of the two enable inputs which latched the output high, as expected. The output signal was presented to the enable input of the counter which began to count. The waveforms observed and recorded at QC and QD are shown in Figure 41a.

When the counter count reaches 15, the inverted Ripple Carry Out signal is presented to pin 1 or pin 13 on the latch, clearing it. The latch output goes low and disables the counter. The latch output going low also clears the counter on the next rising clock edge. When the counter is cleared, the RCO output is negated and the counter resumes counting since the latch input is still high. At this point, the counters run continuously and are unsynchronized. The latch output waveform, which is also the inverted counter RCO output, is shown in Figure 41b.

The latch and counter arrangement was further tested for the synchronization of the counters on each start bit. The

data input waveform from the HP-150 is simulated by a +9V/-9V 20 kHz square wave. The input to the latch after inversion and conversion by the MAX 232 is a +5V/OV pulse with a 50 us period and fifty percent duty cycle. This pulse form simulates a 40 kilobaud RS-232 signal (01010101...) converted to TTL. As can be seen from Figure 41c, the latch output is high for 15 clock pulses (15 us), at most, following the leading edge of the start bit (+9V, RS-232 signal). Then the latch output goes low, disables and clears the counter and remains low until the next high pulse. (Note: The input waveform in Figure 41c is the simulated RS-232 mark/space waveform; the input to the latch is the inverted TTL waveform which is not shown.)

Both sides of the pleisiochronous interface were tested to ensure that a low TTL signal cleared the latches and counters and that a high TTL signal started the counters. Both latch and counter circuits functioned properly.

The multiplexer and demultiplexer were then connected into the circuit shown in Figure 36. The interface was tested for end-to-end operation by presenting the simulated data signal (described above) through the MAX 232 to the latch on the transmit side and through the CAFs and a F/O cable to the distant latch as shown in Figure 28. The inputs to the control signal multiplexer were loaded with specific control signal combinations. The output channels were observed during transmission of the simulated data signal to

ensure that the same control signal that was being transmitted was being received. The control signals, both high and low, were accurately multiplexed and demultiplexed during this test. Two separate crystal oscillators were used to clock the multiplex and demultiplex channel selection. Because these oscillators are not synchronized, the multiplexing/demultiplexing cannot be started simultaneously. Phase "glitches" approximately one clock pulse wide were observable on the demultiplexer output channels.

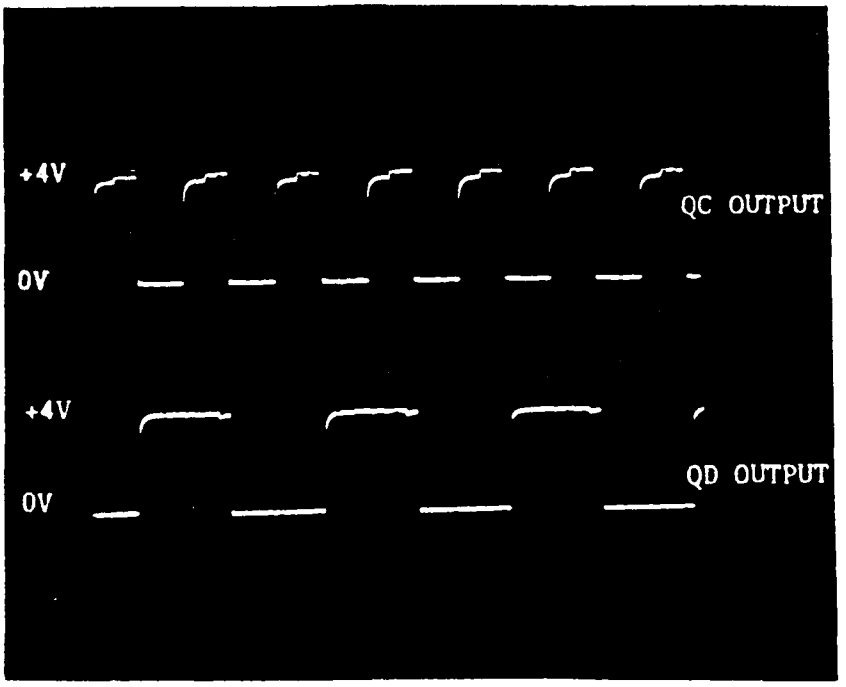


Figure 41a. QC/QD Counter Output Waveforms

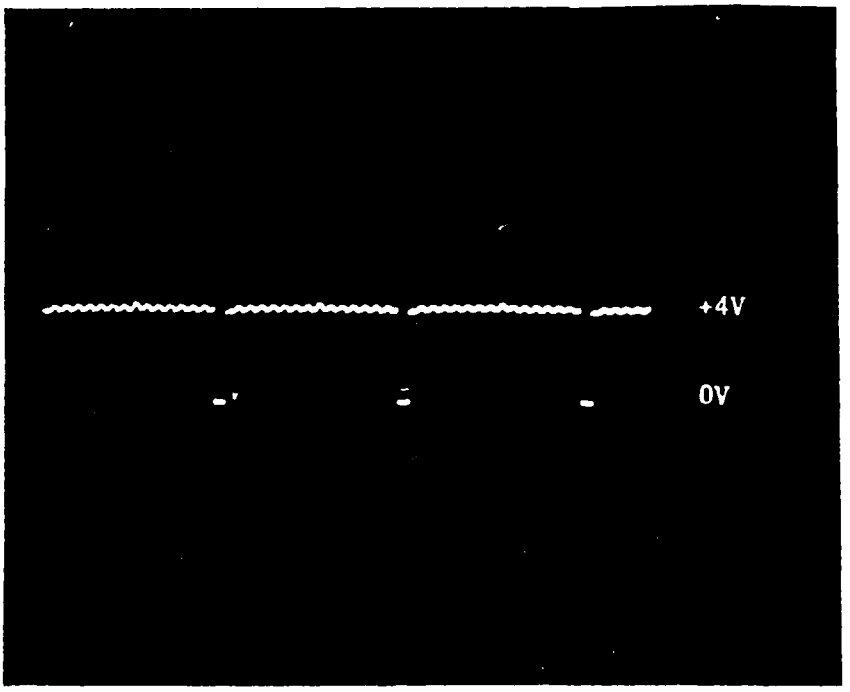


Figure 41b. Latch Output Waveform

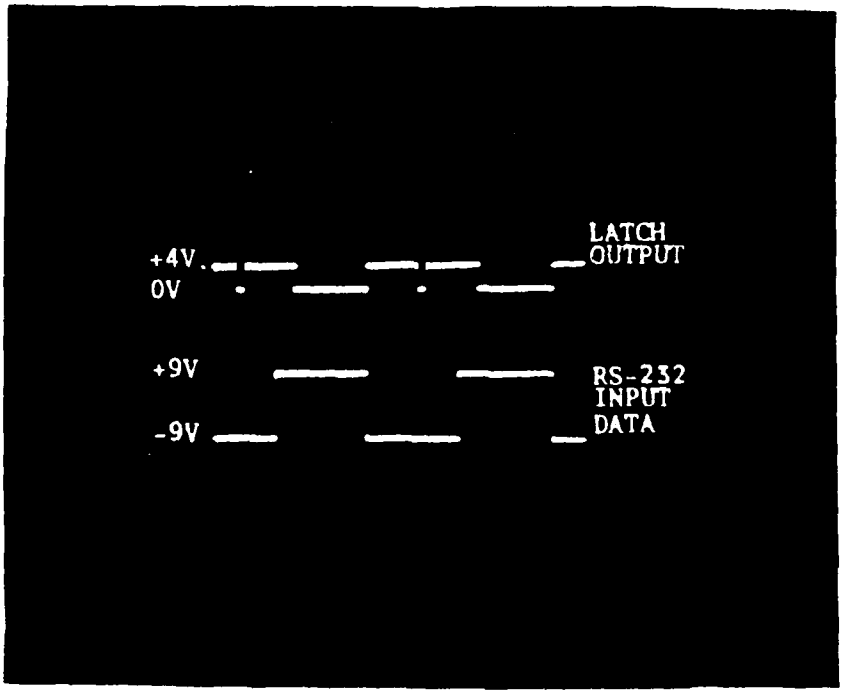


Figure 41c. Input and Output Waveforms for Start Bit Synchronization of the Counters

V. OPERATIONAL TEST AND EVALUATION

Following the test of each building block of the circuit and integration of the building blocks to create the end-to-end system, an end-to-end test was conducted to verify the total capability.

A. TEST PROCEDURE

The HP-150s were configured for data transfer as previously described using the DSN LINK/MONITOR Software. The end-to-end circuit was established by connecting the fiber optic duplexer and the CAFs into the thesis circuit as shown previously in Figures 36 and 18.

Two different files were selected for transfer to test the system capability. One was a 4352 byte binary file, "message.mon", which is found on the DSN LINK disk. The other was a binary drawing file ("picnic.gal", copied from MAC-CAD), 15058 bytes long.

B. TEST RESULTS

Both files were successfully transferred repeatedly at 19.2 kilobaud. Negating the Request to Send control line on either HP-150 while it was receiving caused the Clear To Send input at the transmitting HP-150 to receive the waveform of Figure 38c. When this was done, data transmission was halted. Similarly when the Data Terminal Ready control line on the receiving HP-150 was negated, the Data Set Ready input at the

transmitting HP-150 received the waveform of Figure 38c. Data transmission was also halted in this case. Upon return of the control line to its original state, data transfer recommenced and file transfer completed successfully. Even when data transmission was halted repeatedly during file transfer, the file transfer was successful and error free.

Following each file transfer, the origin file and the destination file were compared using a file comparison program, "fc", which is available on HP's Advanced Programming Tools Disk. Origin and destination files were identical in each case. If a difference exists between the origin and destination files, the program issues a message which tells which bytes are different and itemizes those differences. The "fc" software was verified by editing a test file and comparing it to the unedited file. The differences were itemized correctly.

When the file transfer is successful, the DSN LINK and DSN MONITOR screens should look similar to Figures 9 and 10, previously shown. (The only differences should be the name of source and destination files and the number of bytes and records transferred in a specific example).

VI. EXPANSION OF CONCEPT

This chapter explores possibilities for extending the capabilities of the interface circuit previously described. Extension of the interface circuit capabilities and optimization of the design would logically include transmission of data at the highest possible rate, extension of the maximum link length, reduction of the number of fiber lines necessary and increase in the number of control signals multiplexed. Refinement of the interconnect design to apply to generic RS-232 devices as opposed to the specific HP-150-to-HP-150 application addressed in this thesis is also desirable. Each of these considerations is addressed in this chapter from either a practical or theoretical standpoint. Some experimentation was performed and the results are presented in this chapter. One circuit enhancement was designed for the regeneration of control signal waveforms. That circuit was constructed and tested in conjunction with the thesis circuit. Results are included in this chapter.

A. DATA TRANSMISSION

For this thesis experiment, the data was transmitted at 19.2 kilobaud, which is generally the limiting data rate for the RS232-C Serial Asynchronous Interface [Ref. 11:p. 165]. It is also the highest data rate that can be selected from the menu on the HP-150 configuration screen (previously shown

in Figure 6). An increase in the data transmission rate using this thesis interface is potentially achievable. The limiting data rate for the CAF F/O Receiver/Transmitter electronics is specified as 20 Mbps [Ref. 1]. The limiting factor on the overall data transmission rate, however, is the highest frequency RS-232 signal which can be converted to TTL levels by the MAX 232 chips and reconverted from TTL to RS-232 levels.

The limiting data rate for this thesis circuit was established by applying a square wave with RS-232 characteristics (+9V, -9V) to the MAX 232 RS-232 inputs and increasing the frequency of the square wave while monitoring the corresponding TTL outputs for degradation to the point where logical 1 and 0 levels were not maintained. A TTL characteristic waveform was applied to the TTL inputs and the RS-232 outputs were monitored to establish the limiting data rate for the reverse conversion.

The limit for TTL/RS-232 conversion is approximately 80-85 kHz or 170 kilobaud, above which conversion is unreliable. Specifically, mark and space voltage levels for EIA RS-232C signals did not result from the conversion. The limit was different for RS-232-to-TTL than for TTL/RS-232. RS-232-to-TTL conversion is reliable up to a limiting data rate of about 2 MHz or 4 Mbps, above which logical 1 TTL voltage levels could not be obtained.

As the MAX 232 chip is intended for conversion of RS-232 signals at typical data rates, the manufacturer does not provide specifications on the limiting data rates. The limiting rates identified above must be recognized to be for particular devices, tested out-of-circuit, with a particular signal generator input. Still, the limiting data rate of 19.2 kilobaud could be at least quadrupled without stretching the capabilities of the MAX 232 conversion chip. Further development effort in this area is recommended.

B. ENHANCEMENTS TO DESIGN

As previously discussed, only two control signals from the RS-232 interface of the HP-150 terminals were multiplexed, transmitted, received and demultiplexed. As can be seen from Figure 36, there are two unused inputs on the 74LS153 multiplexer and two unused outputs on the 74LS155 demultiplexer. Obviously, the number of control signals which can be multiplexed and demultiplexed can be increased to four in each direction. Note, however, that the MAX 232 chips have only one unused RS-232-to-TTL and one unused TTL-to-RS-232 conversion line remaining. This limits capacity of the existing circuit to three control signals in each direction.

Additional control signals would require more MAX 232 converter chips and replacement of the four-to-one multiplexers/one-to-four demultiplexers with eight-to-one multiplexers/one-to-eight demultiplexers and an additional

select line from the 74LS163 counters. A commensurate increase in the circuit complexity and in timing and synchronization difficulty logically follows.

The control signals multiplexed in this thesis were high (+9V) or low (-9V) waveforms. The output of the 74LS155 demultiplexer (high unless selected, then true to input) causes an inaccurate reproduction of the control signal at the control input to the distant HP-150 when a -9V, RS-232 level, control signal is transmitted. While this "non-true" waveform was sufficient to inhibit data transmission by the HP-150 as desired, it is likely that this is a peculiarity of the HP-150 interface and may not work for other RS-232 interfaces. Therefore, recreation of the exact control waveform is desirable for wider application of the interface circuit. To that end, a control signal restoration circuit for RS-232 control signals was designed and tested.

A circuit for two control lines is shown in Figure 42. The NE-555 timer is configured in the monostable mode [Ref. 20:p. 5-25]. The pin connections and the function table for the NE-555 timer are provided in Figures 43a and 43b.

When the control signal is high, the trigger input is high and hence has no effect. The threshold voltage rises toward Vcc as the 1 uF capacitor charges through the 100K resistor (T = RC = 0.1 sec). When threshold voltage reaches 2/3 Vcc, the output goes low (assuming that it has been high) and the discharge terminal is grounded inside the NE-555

timer, discharging the 1 uF capacitor. As long as the trigger voltage (the demultiplexer output) stays high, the NE-555 timer stays in the reset state and the latch stays cleared. If the control signal is now negated (goes low), even briefly, the NE-555 trigger voltage drops below 1/3 Vcc and the timer is SET making its output high and floating the discharge terminal. The low output of the demultiplexer is inverted and caught and held by the latch. The output of the latch stays high for 0.1 sec until the NE-555 threshold voltage rises to 2/3 Vcc and the latch is again cleared. The latch stays cleared until next time the trigger voltage falls below 1/3 Vcc [Ref. 20:pp. 5-21 to 5-25].

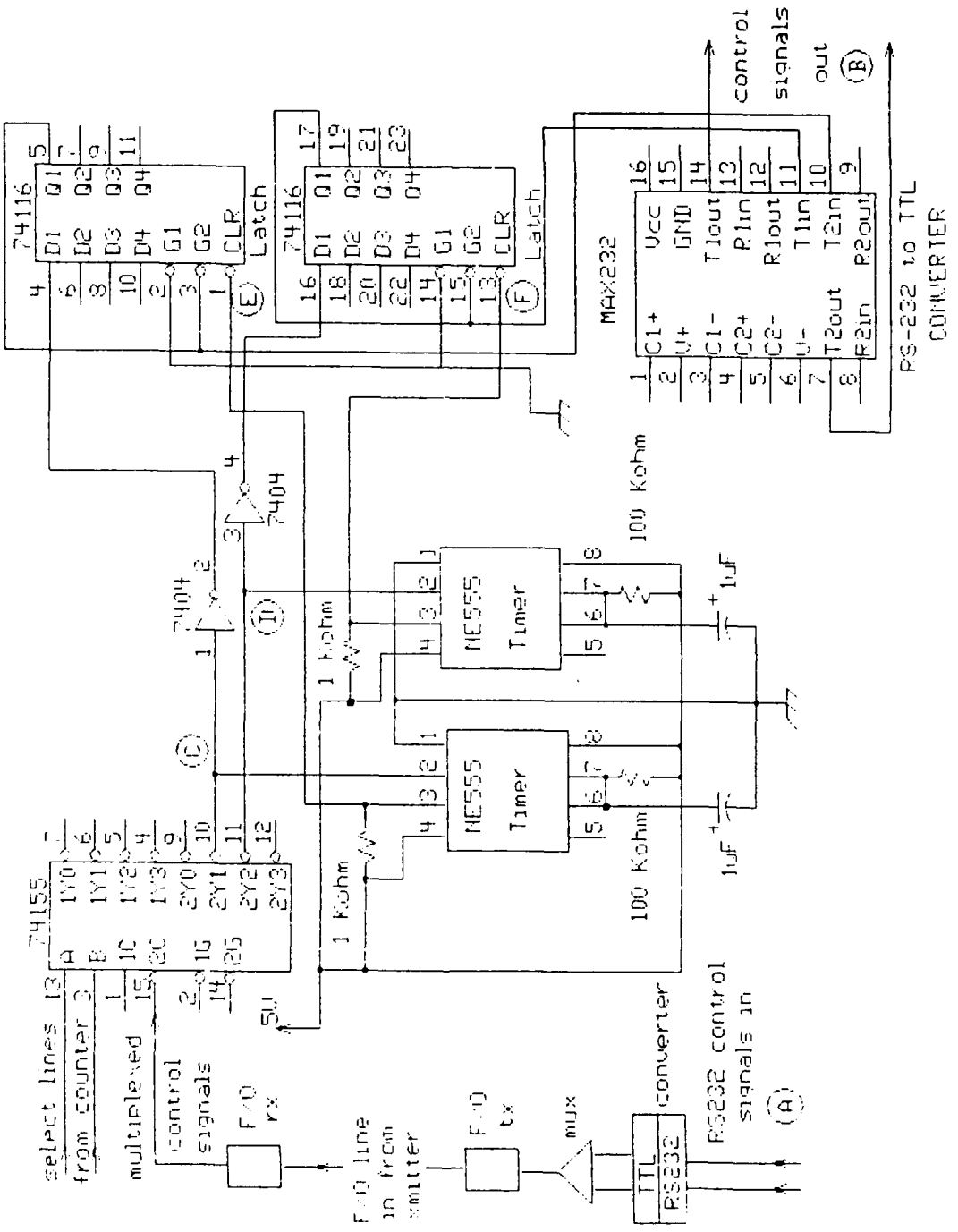


Figure 42. Mark/Space Control Signal Regeneration Circuit

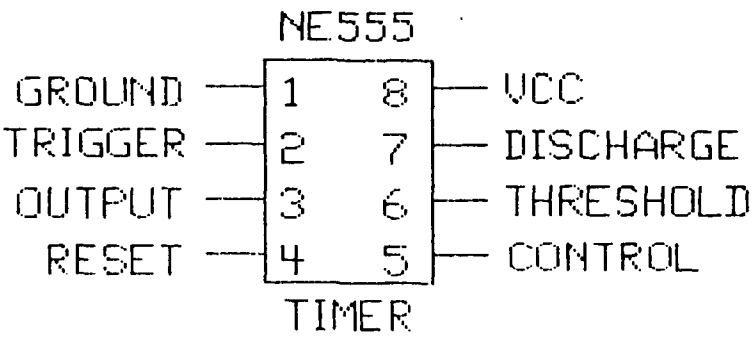


Figure 43a. NE-555 Pin Connections
[from Ref. 20:p. 5-21]

RESET	TRIGGER VOLTAGE	THRESHOLD VOLTAGE	OUTPUT	DISCHARGE SWITCH
Low	N/A	N/A	Low	On
High	< 1/3 V+	N/A	High	Off
High	> 1/3 V+	> 2/3 V+	Low	On
High	> 1/3 V+	< 2/3 V+	as previously set	

Figure 43b. NE-555 Function Table
[From Ref. 20:p. 5-22]

When the control signal is continuously low, the output from the latch will be high with low pulses at 0.1 second intervals. The high output of the latch is inverted by the MAX 232. The true low control signal with high spikes at 0.1 second intervals is presented to the HP-150. These spikes which have been inverted and converted by the MAX 232 are about 12 us wide and approximately +7.5V high. The spikes are ignored by the HP-150 since they do not provide the continuous high control signal level necessary to enable data transfer. When the control signal returns to its high state, the output of the timer goes low within 0.1 seconds clearing the latch.

Sample input and output waveforms for points A and B on Figure 42 are given in Figure 44a which shows high and low control signal outputs following high and low control signal inputs. The high spikes are not discernable on the low output signal from the MAX 232 shown in Figure 44a. The trailing edge of a high spike on a low control line is shown in Figure 44b.

The circuit of Figure 42, while allowing restoration of simple control waveforms, does complicate the circuitry as one dual latch and two timers are required for each two control lines. Notice that the "time-out" on the NE-555 timer shown in Figure 42 is set at one-tenth of a second. With

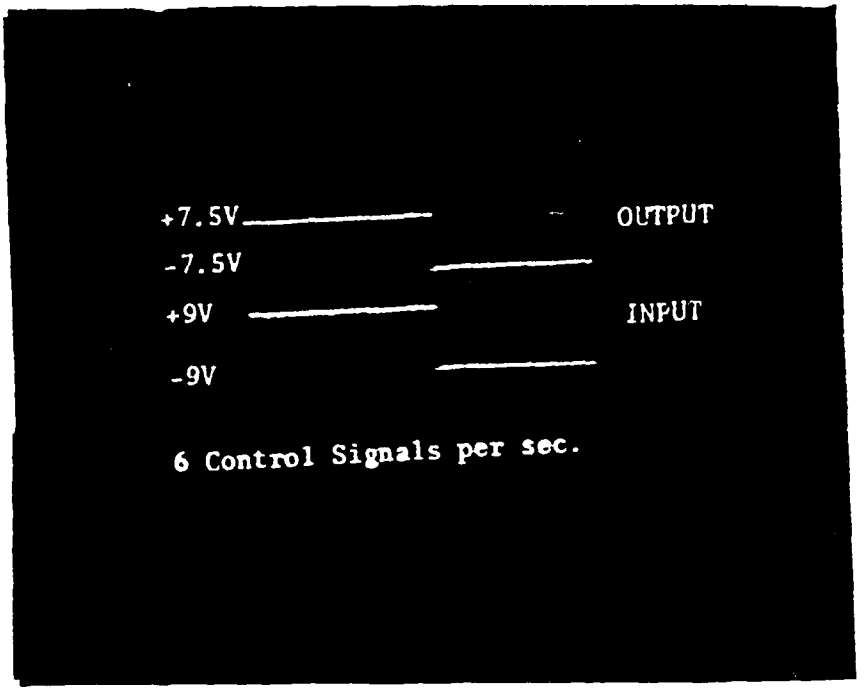


Figure 44a. Input/Output Waveforms for the Circuit of Figure 42

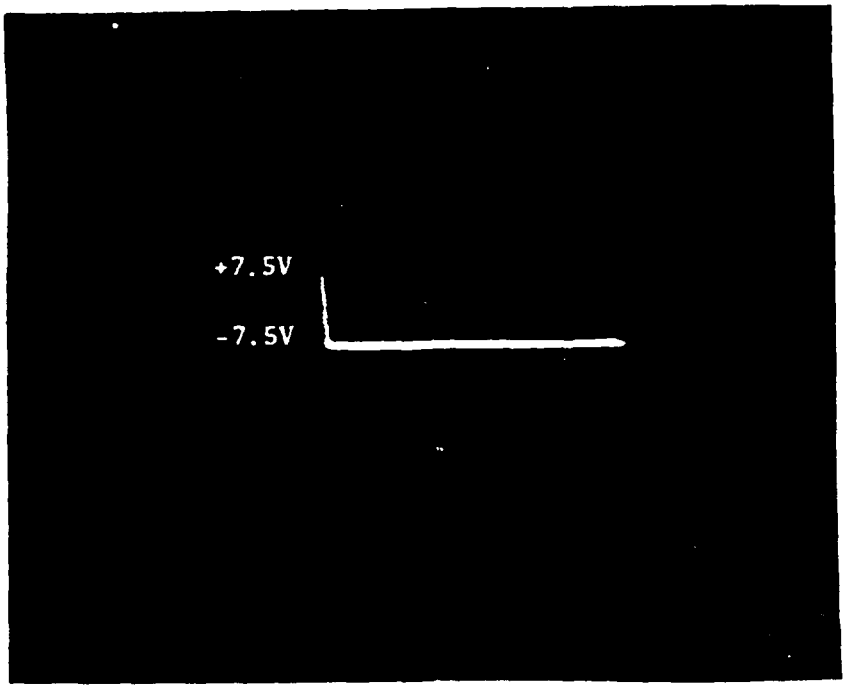


Figure 44b. Low (-7.5V) Control Signal with Trailing Edge of +7.5V Spike

this "time-out" it is possible for a control line to change and the change not be detected for up to that length of time. At 19.2 kilobaud, many characters could be lost in that one-tenth of a second. The missing pulse detector circuit of Figure 45 with a "time-out" of approximately 4 us will eliminate this anomaly. The "time-out" is short enough that a control line cannot change without immediate detection. When a low pulse on the control line is detected, the transistor discharges the capacitor, preventing the output from changing. When the control signal returns high, the low pulse disappears and the timer output changes. The circuit of Figure 42 will function in a greatly improved manner when the NE-555 missing pulse detector is connected at points C, D, E, and F in place of the existing NE-555 one-shot multivibrator.

The missing pulse detector circuit also eliminates the high spikes at 0.1 second intervals that occurred in the previous circuit when the control signal for the channel was continuously negated. One further anomaly exists in the restoration circuit of Figure 42. A low "glitch" resulting from the end-to-end phase synchronization difference between the counters will be caught and latched through to the output. If this latched "glitch" lasts longer than 2 or 3 us it can be converted by the MAX 232 and interpreted as a low control signal which will halt data flow. This anomaly cannot be eliminated in this circuit.

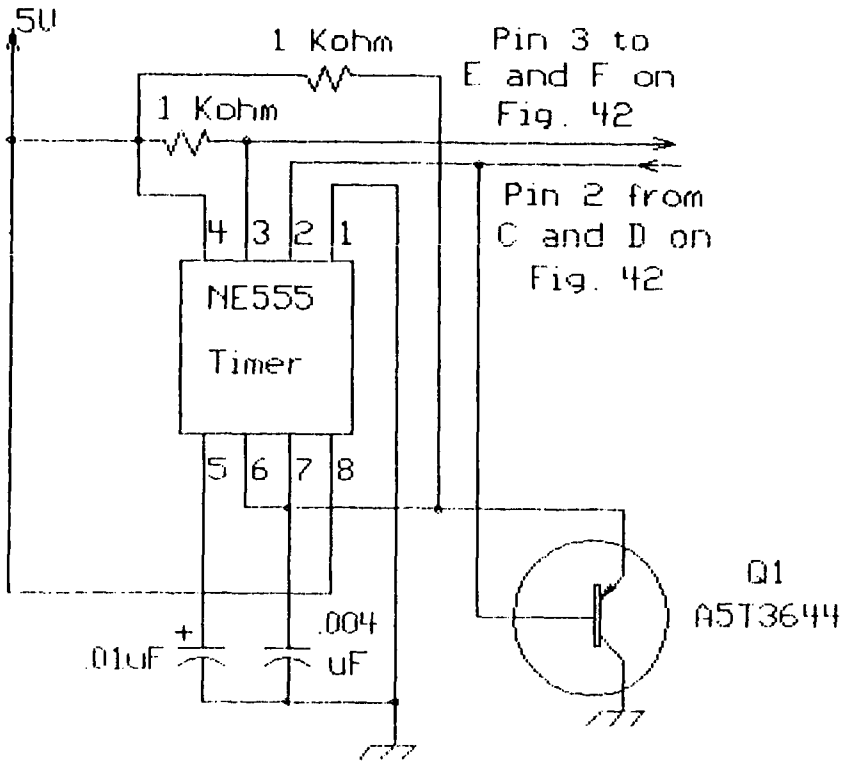


Figure 45. Missing Pulse Detector
[from Ref. 20:p. 5-25]

Other methods of restoring the control signals, such as sample and hold circuits for the demultiplexer outputs during appropriate output intervals, are perceived to be part of a future development effort. A sample and hold circuit could be implemented in a straightforward manner by presenting each demultiplexer output to the D input on a 74LS74 flip-flop and clocking the flip-flop with the "anded" input of the system clock and a count detector. The count detector can be implemented by "anding" the appropriate counter outputs or, more elegantly, with a 4 x 16 decoder circuit attached to the counter outputs. Thus, each demultiplexer channel would be sampled when selected and the value latched until the next

sample was taken. The control signal out of the demultiplexer would then be the true control signal that was transmitted. The inversion in the HFBR 1402/2402 link must still be accounted for but can be done simply by using the C1 input to the 74LS155 demultiplexer. A sample and hold circuit would also eliminate the phase "glitches" on the demultiplexed control lines.

Use of the start bit for counter (clock) re-synchronization was sufficient for the HP-150 interconnect. Transmission of a synchronization pulse which sets the latch and clears the counter periodically would accomplish the same function as the start bit of the data frame. Such a pulse could be "piggy-backed" on the data line. If the pulse was narrow (1 us), the MAX 232 would not convert it into an RS-232 signal for reasons discussed previously. Transmission of the synchronization pulse once each milli-second would re-synchronize the multiplex and demultiplex counters and have no effect on the RS-232 data signals. Configuration of an NE-555 in the astable mode with the desired pulse width and repetition rate at the output is the easiest way to implement this enhancement. Additional changes to the original circuit would be required for this implementation since the existing design requires a synchronization pulse of 16 us or longer.

Implementation of all of these refinements and enhancements is perceived to result in a universally

applicable RS-232 fiber-optic interconnect with provision for active handshaking.

C. LINK OPTIMIZATION

This section contains the theoretical link analysis for the F/O RS-232 interface. Analysis is based on the measured power out of the F/O transmitters, the specified minimum input power for the F/O receivers, the calculated loss for the cable utilized, the measured loss for the F/O duplexer and the typical loss for couplers/splices. This section also suggests one possible approach to the reduction of the number of F/O lines using F/O WDM techniques.

To determine the maximum F/O link length using the F/O components currently incorporated in the thesis interface, the optical output power of each transmitter was measured and recorded. The following coupled power out values were measured using the Photodyne 22XLA F/O multimeter for the configuration shown in Figure 46:

TABLE 7
MEASURED OPTICAL POWER

F/O TRANSMITTER	COUPLED POWER OUT
HFBR 1402 (1)	-10.5 dBm
HFBR 1402 (2)	- 9.0 dBm
CAF (1)	-11.1 dBm
CAF (2)	-12.5 dBm

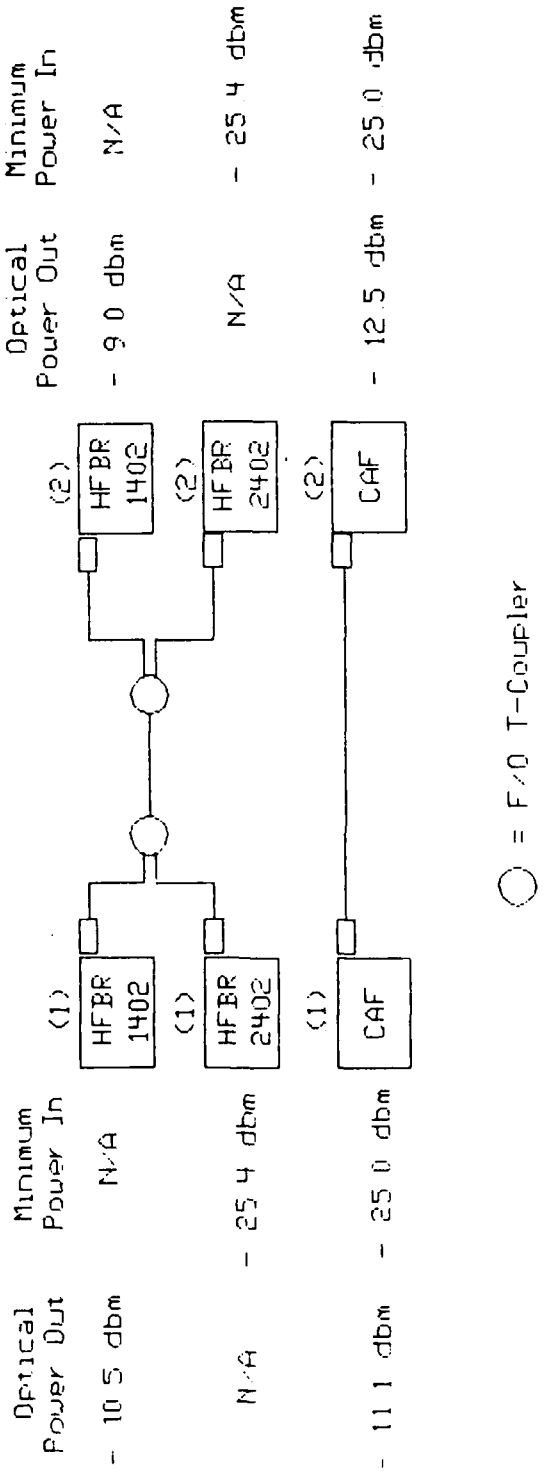


Figure 46. Optical Power Budget Calculation Configuration

The minimum optical power at the F/O receivers was determined from the equipment specifications. The HFBR 2402 F/O receiver requires a minimum input power of -25.4 dBm [Ref. 2] and the CAF F/O receiver requires a minimum input power of -25 dBm [Ref. 1]. Using the input and output values of optical power from Chapter V, the loss in the duplexer can be established as 6.4 dB (worst case, including coupling). This value will be required to calculate the maximum link length. The loss that the link will tolerate and still operate is

$$\text{Losses (dB)} = 10 \log (P_t/P_r) \qquad (6.1)$$

where P_t = power out of the transmitter
P_r = minimum power required at the receiver [Ref. 21:p. 258].

Alternatively, this loss can be expressed as

$$P_t \text{ (dBm)} - P_r \text{ (dBm)} = \text{Losses (dB)}. \qquad (6.2)$$

Using the worst case values for the HFBR 1402 to HFBR 2402 link, this results in

$$-10.5 \text{ dBm} - (-25.4 \text{ dBm}) = 15.1 \text{ dBm}. \qquad (6.3)$$

Therefore, 15.1 dB is the acceptable system loss for a marginally operating system. For the CAF-to-CAF system, the acceptable system losses are

$$-12.5 \text{ dBm} - (25.0 \text{ dBm}) = 12.5 \text{ dB}. \qquad (6.4)$$

The losses in the link can be expressed as

$$\text{losses (dB)} = \alpha_o L + l_t + n_{ls} + 2n_{lc} + l_r + l_a + l_m \qquad (6.5)$$

where α_o = loss/kilometer of fiber

L = length of link
l_t = coupling loss at transmitter
n_{ls} = number of splices times splice loss
$2n_{lc}$ = number of connector joints times coupler loss

l_r = coupling loss at receiver
l_a = aging loss
l_m = link margin [Ref. 21:p.258].

For this system l_t and l_r were included in the coupled output power of the transmitters. The aging loss, l_a, and link margin, l_m are assumed to be zero for a marginally operational system. These losses are taken into account in separate link analysis. All splices (normally one splice per km) are assumed to be fusion splices at 0.1 dB/splice. The fiber optic duplexer loss of 6.4 dB (end/end, worst case, including couplers) is accounted for in the HFBR 1402 to 2402 link as l_{dpx}. The fiber optic cable is 100/140 micrometer cable with a typical loss coefficient, α_o= 5.5 dB/km [Ref. 22:p. 4-93].

For the HFBR 1402 to 2402 link:

$$\text{losses (dB)} = l_{dpx} + \alpha_o L + n_{ls}. \quad (6.6)$$

Substituting:

$$15.1 \text{ dB} = 6.4 \text{ dB} + 5.5 \text{ dB/km} * L(\text{km}) + n(.1\text{dB}). \quad (6.7)$$

Rearranging:

$$15.1 \text{ dB} - 6.4 \text{ dB} = 5.5 \text{ dB/km} * L(\text{km}) + n(.1\text{dB}). \quad (6.8)$$

Assuming 1 splice/km

$$8.7 \text{ dB} = 5.6 \text{ dB/km} * L(\text{km}). \quad (6.9)$$

(Note: there is one less splice than there are km but the 0.1 dB difference is negligible.)

Solving for L in km:

$$\frac{8.7 \text{ dB}}{5.6 \text{ dB}} = 1.5 \text{ km.} \qquad (6.10)$$

Solving for the CAF to CAF link length which does not involve the F/O duplexer gives a possible link of over two km in length using the same derivation. The HFBR 1402 to 2402 maximum link length therefore determines the maximum possible separation between terminal devices.

Recall that no link or aging margin was incorporated into the above calculations. Recalculation of the length using typical values of 3 dB for l_a and l_m yields:

$$8.7 \text{ dB} = 5.6 \text{ dB/km} \quad L(\text{km}) + 3 \text{ dB} + 3 \text{ dB}. \qquad (6.11)$$

Solving for L gives L = 480 meters. (Note: no splices would be necessary for this link length but again the 0.1 dB is negligible.)

The link length could be extended if required through the use of more powerful optical transmitters (i.e., lasers), the use of single-mode, low-loss fiber, and/or the use of more sensitive detectors (i.e., avalanche photodiode (APD) receivers) [Ref. 21:pp. 256-267]. Pursuit of these enhancements is left to future research.

Another way that the interface can be improved is by reducing the number of F/O lines used for the interface. Through WDM and F/O duplexing, that number has been reduced from four to two. There exists the potential, through further WDM, to reduce the number of F/O lines to one. The

types of devices available for implementation of such WDM are either angularly dispersive devices such as prisms or filtering devices such as dichroic filters. For three wavelength use of a single fiber, an optical bandpass filter is required in addition to the dichroic filter already employed. Such an optical bandpass filter would be centered around the HFBR 1402/2402 operating wavelength, 820 nm, and would reject the CAF wavelengths of 865 and 730 nanometers. This type of filter could be employed to get all three wavelengths into and out of the same fiber. The actual mechanics of this is left to future study.

VII. CONCLUSIONS

This chapter contains a discussion of the results of the thesis research in respect to problems addressed and resolved during the thesis research. It also contains information on the perceived benefit of the study and possible military applications in which the concept would be advantageous. Potential areas for future thesis research based on this thesis are also discussed in this chapter.

A. PROBLEMS ADDRESSED AND RESOLVED

The primary goal of this research was to design, implement and test an RS-232 fiber optic interface which would provide not only for data transmission from one DTE to another, but would also make provision for the simultaneous transmission of handshaking information necessary to control that data flow. The goal was to include control signals without merely replacing each RS-232 control line with a F/O line and the associated electro-optic equipment. In order to achieve the primary objective, resolution of several subsidiary problems became necessary. The control signals had to be successfully converted from RS-232 signal levels to TTL levels, multiplexed, converted to optical signals, reconverted to TTL, demultiplexed and reconverted to RS-232 format. Each of these problems was addressed and resolved as

previously described in Chapter III, Design, and Chapter IV, Engineering Test and Evaluation.

Other subsidiary problems concerned the maximum possible reduction of the number of fiber optic lines used. If the null modem interface is replaced with fiber on a line by line basis, not including ground lines, six fiber optic lines are required. Use of control signal multiplexing reduced this number to four, fiber optic duplexing of the transmit/receive lines for the handshaking signals reduced the number of F/O lines to three and WDM of the data transmit/receive lines reduced the final interface configuration to two F/O lines.

The most significant subsidiary problem in terms of getting the interface to work was the synchronization of the multiplex/demultiplex of the control signals. Use of a relatively unique approach for DTE/DTE communication, a pleisiochronous interface, enabled the control signals to be multiplexed, demultiplexed and to appear on the proper handshaking lines at the distant DTE during data transfer.

Another subsidiary problem addressed was that of recreation of true high and low (mark and space) control signals at the distant DTE. As previously explained, the requirement for this arose from the nature of the output on the demultiplexed channels of the 74LS155 demultiplexer. Two approaches to resolution of this problem were explained in Chapter VI. With the resolution of all subsidiary problems for the HP-150-to-HP-150 interface, the thesis goal of RS-232

format data transmission over a F/O interface, employing active handshaking from DTE to DTE was achieved.

B. BENEFIT OF STUDY

The benefit of the study lies primarily in the demonstration of an RS-232 interface for DTE/DTE communication over the media of fiber optics in a fairly straightforward manner. The benefits of the use of F/O as a transmission media are well known and widely published. Just to name a few, F/O cable is light, small and cost-effective compared to copper cable. It is resistant to jamming, resistant to electromagnetic interference, resistant to Electromagnetic Pulse (EMP) and High Altitude EMP (HEMP). It exhibits little crosstalk, is capable of supporting enormous data rates and has low transmission loss [Ref. 23:p. 14].

The military applications of the concept developed in this thesis research are myriad. Among them are permanent intrabase and interbase data communications links for peacetime use, as well as rapidly and easily deployable tactical data communications links within and between field locations. RS-232C is the standard currently employed for the interface of DTE, DCE and peripherals [Ref. 11:pp. 167-168]. The DoD community specifies this standard almost exclusively when writing specifications for Requests for Proposal (RFPs) for such equipment. The potential utility of the thesis concept is evident.

In the event that DTE to DTE, DCE, or peripheral data communications is required, the use of a fully RS-232 capable F/O interface (including handshaking) is perceived to enhance the quality, survivability, security, performance capability and cost effectiveness of such communications [Ref. 22:pp. 145-150]. Geographical dispersion of field command posts, remoting of data gathering and processing Signal Intelligence systems, resistance to interference or intrusion, as well as reduction in electrical emanations are among the enhancements realizable with F/O linked RS-232 DTE/DTE.

One application of particular interest is remote communications with tethered vehicles or Remotely Piloted Vehicles (RPVs). An in-progress project at the Naval Postgraduate School is utilizing a DTE/DTE communications link to do control surface analysis on an underwater vehicle. Use of the concept developed in this thesis would allow a very lightweight F/O interface cable to be employed, thereby minimizing the effect of cable drag on the submersible.)

Another application of interest is HEMP-protected data communication between two shielded enclosures in a specific command center. A current USAISC project requires just such an interface between Technical Control Facility (TCF) equipment in one enclosure and subscriber data communications equipment in another enclosure. The civilian applications and benefits of the thesis concept and design parallel the military ones discussed above.

C. POTENTIAL AREAS FOR FUTURE THESIS RESEARCH

During the progress of this thesis several areas of endeavor relating to the primary research goal were discovered. Those have been discussed in previous chapters but are reiterated here in summary form. One future thesis project is possible in the area of extension of link length through the incorporation of high power laser F/O transmitters and highly sensitive APD detectors. Another area of link optimization, that is perceived as a thesis possibility, is the use of WDM techniques to reduce the interconnecting fiber lines to a single line (i.e., to get all three frequencies of light employed to propagate on a single fiber without significant interference). Perhaps the most utilitarian extension of this thesis effort is the pursuit of the hardware refinements described in Chapter VI. Implementation of the enhancements in synchronization, control signal restoration and circuit initialization would result in a widely applicable RS-232 F/O interconnect with full handshaking capability.

To facilitate research in these or related areas, printed circuit boards (PCBs) for the circuit of Figure 36 have been produced. A set of working PCBs is available in the Optical Electronics Lab at the Naval Postgraduate School. The masks for the PCBs (two sided) are shown in Figure 46 and Figure 47. A future thesis effort related to the development of the interface designed in this thesis should address system

implementation costs and tradeoffs. All documentation (except library and personal texts) is available in the Optical Electronics Lab.

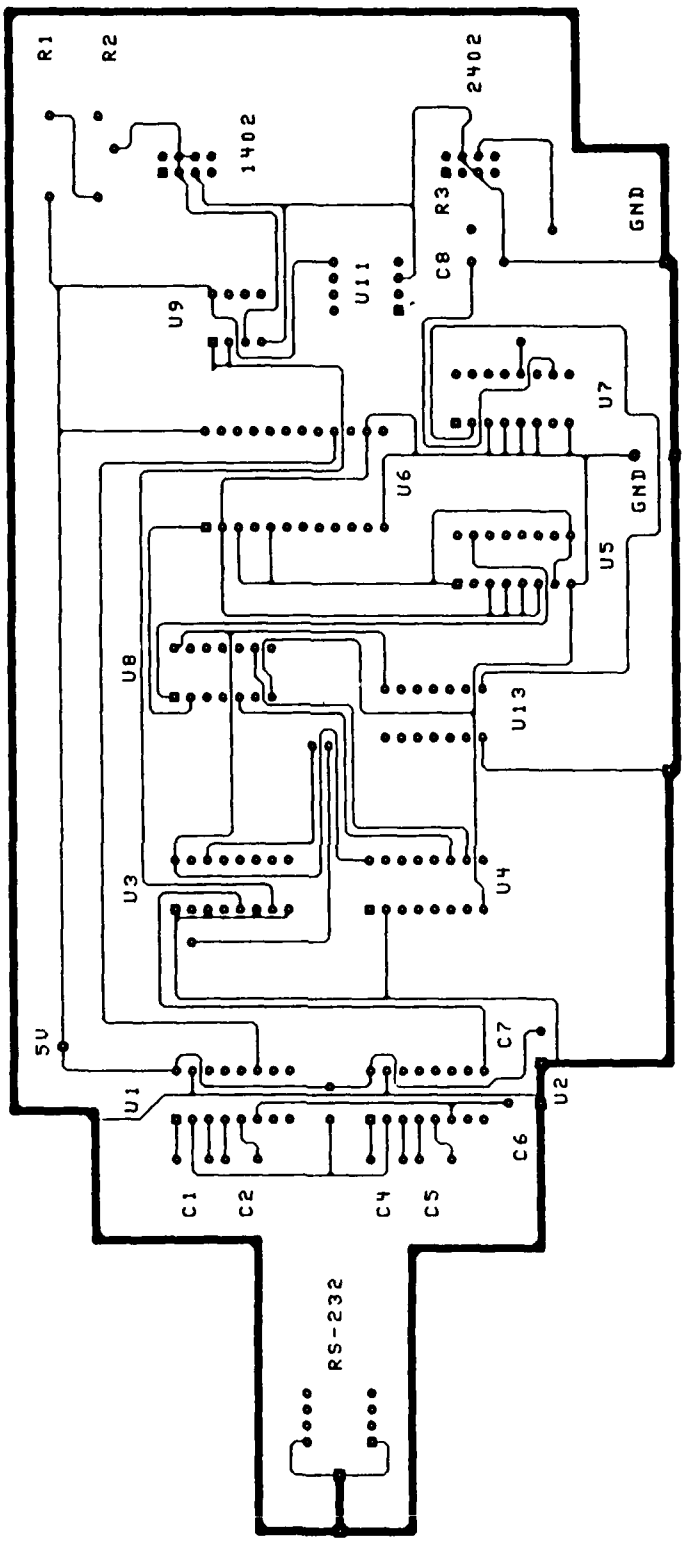


Figure 47. PCB Side 1 - Mask

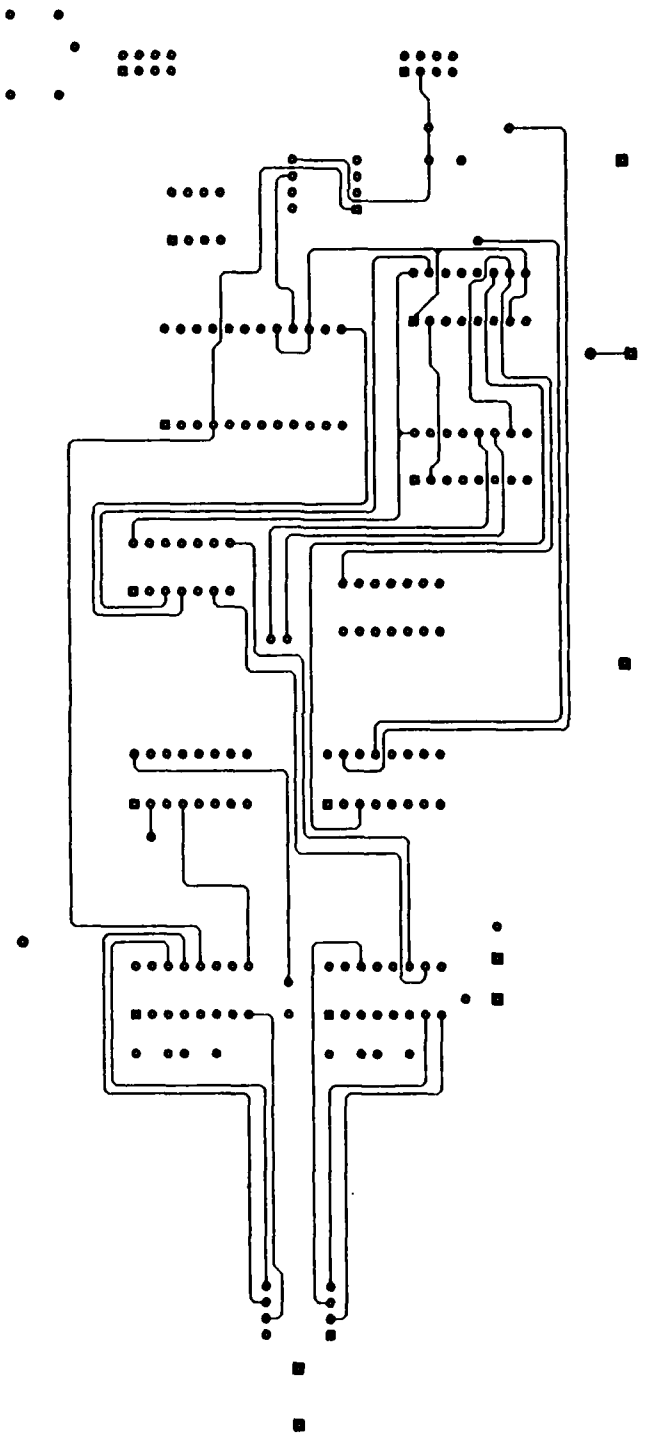


Figure 48. PCB Side 2 - Mask

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